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Thermal Characterization of Nanostructures and Advanced Engineered Materials

A Dissertation submitted in partial satisfaction
of the requirements for the degree of

Doctor of Philosophy

in

Electrical Engineering

by

Vivek Kumar Goyal

December 2011

Dissertation Committee:

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Dedicated

to my parents

ABSTRACT OF THE DISSERTATION

Thermal Characterization of Nanostructures and Advanced Engineered Materials

by

Vivek Kumar Goyal

Doctor of Philosophy, Graduate Program in Electrical Engineering
University of California, Riverside, December 2011
Dr. Alexander A. Balandin, Chairperson

Continuous downscaling of Si complementary metal-oxide semiconductor (CMOS) technology and progress in high-power electronics demand more efficient heat removal techniques to handle the increasing power density and rising temperature of hot spots. For this reason, it is important to investigate thermal properties of materials at nanometer scale and identify materials with the extremely large or extremely low thermal conductivity for applications as heat spreaders or heat insulators in the next generation of integrated circuits. The thin films used in microelectronic and photonic devices need to have high thermal conductivity in order to transfer the dissipated power to heat sinks more effectively. On the other hand, thermoelectric devices call for materials or structures with low thermal conductivity because the performance of thermoelectric devices is determined by the figure of merit $Z=S^2\sigma/K$, where S is the Seebeck

coefficient, K and σ are the thermal and electrical conductivity, respectively. Nanostructured superlattices can have drastically reduced thermal conductivity as compared to their bulk counterparts making them promising candidates for high-efficiency thermoelectric materials. Other applications calling for thin films with low thermal conductivity value are high-temperature coatings for engines. Thus, materials with both high thermal conductivity and low thermal conductivity are technologically important. The increasing temperature of the hot spots in state-of-the-art chips stimulates the search for innovative methods for heat removal. One promising approach is to incorporate materials, which have high thermal conductivity into the chip design. Two suitable candidates for such applications are diamond and graphene. Another approach is to integrate the high-efficiency thermoelectric elements for on-spot cooling. In addition, there is strong motivation for improved thermal interface materials (TIMs) for heat transfer from the heat-generating chip to heat-sinking units. This dissertation presents results of the experimental investigation and theoretical interpretation of thermal transport in the advanced engineered materials, which include thin films for thermal management of nanoscale devices, nanostructured superlattices as promising candidates for high-efficiency thermoelectric materials, and improved TIMs with graphene and metal particles as fillers providing enhanced thermal conductivity. The advanced engineered materials studied include chemical vapor deposition (CVD) grown ultra-nanocrystalline diamond (UNCD) and microcrystalline diamond (MCD) films on Si substrates, directly integrated nanocrystalline diamond (NCD) films on GaN, free-standing polycrystalline graphene (PCG) films, graphene oxide (GOx) films, and

"pseudo-superlattices" of the mechanically exfoliated Bi_2Te_3 topological insulator films, and thermal interface materials (TIMs) with graphene fillers.

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Chapter 1

Introduction

1.1 Thermal Conductivity and Phonons

One of the fundamental properties of solids is their ability to conduct heat. It is usually quantified in terms of thermal conductivity coefficient *K*, given by the Fourier's Law of heat conduction,

$$\dot{Q} = -KA\Delta T \quad [1.1]$$

where $\dot{Q}$ is time rate of heat flow, A is the total cross sectional area of conducting surface, ΔT is the temperature difference, and *K* is the thermal conductivity coefficient [1]. Heat energy can be transmitted through solids via electrons (or holes), lattice waves (phonons), spin waves, electromagnetic waves, or other excitations. In metals electrical carriers conduct the majority of heat, while in insulators lattice waves are the dominant heat carriers. The total thermal conductivity of semiconductor materials is given by

$$K = K_e + K_p \quad [1.2]$$

Where K is the total thermal conductivity, K_e is the thermal conductivity component due to electrical charge carriers and K_p is the thermal conductivity component due to the phonons (lattice vibrations). Phonons are the quanta of lattice vibrations analogous to the

photons, which are the quanta of light. Phonons are quasi-particles having energy ħω and quasi- momentum $p=\hbar q$, which obeys Bose-Einstein statistics [2, 3]. At low temperatures (~0K), these phonons propagate through a perfectly elastic crystal without interfering with one another, but at high temperatures (above room temperature) the momentum is not conserved in the phonon- phonon interaction due to Umklapp process and this introduces thermal resistance which limits thermal conductivity to $1/T$. The lattice part of the thermal conductivity is usually negligible in a metal owing to very high electron component K_e. On the other hand, in semiconductors the conduction of heat is mostly due to lattice vibrations. The lattice vibrations generate waves that can propagate through the insulator/semiconductor, hence transporting thermal energy from one end of the solid to another. Thermal conductivity can be viewed as the result of phonons (quasiparticle) moving from a hotter to a colder region and undergoing collisions with one another or against material imperfections (defects, boundaries, etc.) so that their energy can be transferred in space. These collisions are often referred to by using more general term *scattering*. The mathematical model commonly followed makes use of the kinetic theory of gases, in which: (i) each phonon is modeled as a free moving particle in space with a momentum and an energy, (ii) which is subject to instantaneous collision events with other particles, (iii) the probability for a collision to occur during an interval of time *dt* is proportional to *dt*, (iv) and the particles reach thermal equilibrium only through these collisions. The lattice contribution K_p can be regarded as the thermal conductivity of a phonon gas and can be derived using kinetic theory of gases:

$$K_P = \frac{1}{3}\left(\frac{C_v^p}{V}\right) v_0 \Lambda \qquad [1.3]$$

where $(\frac{C_v^p}{V})$ is the heat capacity per unit volume of the solid considered and v_0 is the average phonon velocity. Λ is the mean free path of a phonon between two consecutive collisions. There are two types of phonon-phonon interactions in crystals. The first one involves normal processes where the overall phonon momentum is conserved: $\vec{k}_1 + \vec{k}_2 + \vec{k}_3 = 0$, where $\vec{k}_1$, $\vec{k}_2$ and $\vec{k}_3$ are the momenta of three interacting phonons. The second type is called umklapp processes where, $\vec{k}_1 + \vec{k}_2 + \vec{k}_3 = n\vec{K}$, where n is an integer, and $\vec{K}$ is a reciprocal lattice vector. Electron and lattice momentum in a crystal is only conserved give or take a reciprocal lattice vector [4]. At very low temperatures, $T << \theta_D$, the average number of phonons tends toward zero. The phonon-phonon scattering becomes negligible (from Bose-Einstein statistics) and the mean free path is determined by the scattering of phonons against the solid imperfections or the solid boundaries [2]. In particular, $K_p \to 0$ when $T \to 0$ and has a T^3 dependence. For higher temperatures, i.e. $T >> \theta_D$, the average number of phonons is proportional to *T*. Thus, phonon-phonon interactions become increasingly dominant as the temperature increases and mean free path ends up being proportional to *1/T*. The thermal conductivity K_p therefore is proportional to *1/T* in this regime [5].

1.2 Thermal Management at Nanoscale

The invention of solid state transistor and subsequent invention of the integrated circuit (IC) has advocated an unparallel technological and economic growth. In the last one decade, the aggressive downscaling of the device size has yielded enormous gains in

terms of speed, energy efficiency, portability, device density and form factor. So far, device engineers have been successful to maintain Moore's Law, which states that the numbers of transistors on an integrated chip will double every year [6]. This law was predicted to last a decade, from 1965 to 1975. In 1975, this slope changed to doubling every 18 months. This has led to both a reduction of the size of transistors as well as an increase in the packing density. The increase in transistor density has also leaded to a significant increase in the power density (heat) in the same area that needs to be removed from the chip [7]. This law has continued for almost half a century and in 2005 was not expected to stop for another decade at least, because the fundamental thermodynamic limits are being reached in critical areas and innovative changes need to be made in both device structures and transistor materials so that the current rate of improvement can be maintained. The variety of novel phenomena that emerge at nanoscale include spatial confinement and quantization of phonon modes [8], decreased phonon group velocity, increased phonon boundary scattering [9], phonon redistribution due to scattering from rough boundaries and interfaces, pronounced thermal boundary resistance, and rarefied phonon gas effect. When the device feature size becomes comparable to the phonon mean-free-path (MFP) then in addition to the Umklapp scattering and Rayleigh scattering, phonon boundary/rough interface scattering emerges as a dominant phonon scattering mechanism. The definition of temperature also becomes very crucial in the scale of phonon mean free path and wavelength [10].

Thermal management has traditionally been a post-chip-making effort. Currently, it starts from the device and circuits packaging level itself. Increased number of

interconnects and decreased transistor feature size lead to an increased thermal resistance of the ICs and the associated difficulties in heat removal [11]. Another phenomenon, which becomes more crucial as photonic device integration increases and the number of layers go up, is the thermal boundary resistance. It occurs when the heat flows in the direction normal to the interface of two materials, a temperature drop may develop due to the acoustic impedance mismatch between the two materials even if the interface is atomically sharp [12].

Another aspect of the nanoscale heat management is related to the increasing demand of the operating speed of electronic devices. Effective means of heat removal are becoming a pressing issue for assuring the reliable performance and longevity of the nanodevices. Detailed knowledge of the mechanisms and physics in heat dissipation is thus essential for assuring superior thermal performance of nanodevices.

1.3 Thermal Boundary Resistance

Thermal boundary resistance (TBR) is defined as the inverse of thermal conductance, *G*, and it is used to describe thermal transport across an interface. TBR is given by

$$R_{Bd} = \left[\frac{\dot{Q}}{A.\Delta T} \right] \qquad [1.4]$$

where $\dot{Q}$ is the heat flow across an interface, A is the unit area and ΔT is the temperature difference between the two sides of the interface. When heat is transferred across an interface between two different materials, there is a temperature discontinuity at the interface. This effect was first observed at the interface between metal and liquid helium [13] but has later also been seen at the interface between two solids [14]. The qualitative differences between the behavior of boundary resistances at solid-solid and solid-helium interfaces can be explained by two limiting models of boundary resistance, the acoustic mismatch model – which assumes no scattering and the diffuse mismatch model – which assumes that all phonons incident on the interface will scatter. The qualitative differences between the behavior of boundary resistances at solid-solid and solid-helium interfaces can be explained by two limiting models of boundary resistance, the acoustic mismatch model – which assumes no scattering and the diffuse mismatch model – which assumes that all phonons incident on the interface will scatter.

Thermal boundary resistance at solid-solid interface plays an important role in the thermal stability of many electronic circuits, micro devices, superconducting devices, and the whole package itself. With the ever-decreasing size of microelectronics, growing applications of super lattices, and development of nanotechnology, effect of thermal resistances between interfaces (solid-solid) on thermal conductivity are becoming increasingly important. In 1952, the first theoretical description of the phenomenon was suggested by Khalatnikov [15]. The description, currently known as the acoustic mismatch model (AMM), predicts poor phonon transport across interfaces when there are large differences in the density and sound velocity for the two interface materials, as is

the case for the interface between liquid helium and most solids. The AMM was extended to solid-solid interfaces by Little in 1959 [12]. More recently, in 1987, Swartz measured TBR for several metal film and dielectric interfaces up to a temperature of 200 K [16]. Swartz found that below 30 K there was good agreement between the model and experiment, but above 30 K the model tended to under predict the measured TBR.

In order to account for the phonon scattering at interfaces, the diffuse mismatch model (DMM) was suggested by Swartz and Pohl [14]. The model assumes that all phonons incident on the interface from both sides are elastically scattered and then are emitted to either side of the interface. The probability for a phonon to be emitted to a particular side is proportional to the phonon density of states (DOS) of the two materials. Inherent to the DMM is that the transport is independent of the interface structure itself and is only dependent on the properties of the two materials. DMM also assumes only elastic scattering takes place at the interface. In the case of low temperature liquid He to solid interfaces the DMM predicts TBR two orders of magnitude lower than the one predicted by the AMM, while for solid-solid interfaces the differences are small [14].

1.4 Overview

The introduction thus far suggests that in order to deal with the problem of increasing hot spot temperatures in scaled down chips and devices, it is crucial to investigate thermal properties of materials at nanometer scale and identify materials and structures in which

thermal properties can be engineered. This dissertation explores the thermal transport in a set of advanced engineered materials and device structures at nanoscale. We begin with the discussion of material properties and device structures investigated in this dissertation (Chapter 2). Chapter 3 discusses the experimental techniques used for thermal conductivity measurements which include two transient plane source techniques and the Raman optic technique. The first metrology tool discussed is the transient plane source (TPS) "hot disk" technique, which can measure the average in-plane thermal conductivity, and the second technique is the optical "laser flash" technique (LFT), which measures the average cross-plane thermal conductivity. Raman optic technique was first developed for measurement of thermal conductivity of graphene [17]. This chapter describes the theory related to each experimental techniques used, the experimental set-up and the sample preparation procedure. In Chapter 4, experimental and theoretical results of thermal conduction in ultrananocrystalline (UNCD) and microcrystalline (MCD) diamond films on Si are presented. Thermal conductivity has been measured for a high temperature range of 25 ^{0}C to 250 ^{0}C. The phonon-hopping model has been envisaged to describe the measured thermal conductivity dependence on temperature. Result shows that although synthetic-diamond/Si wafers are more thermally resistive than Si at *RT*, but they outperform Si at elevated temperatures. It has been investigated that the grain size, diamond film thickness and thermal boundary resistance between film and Si act as important parameters to engineer thermal properties in these advanced engineered materials. In chapter 5, we studied the thermal transport in nanocrystalline diamond/GaN composite wafers for beyond Si high-power, high-temperature electronic devices with

better thermal management. We demonstrated a novel approach to integrate good quality NCD films with GaN at relatively low substrate temperatures (~450 ^{0}C). We experimentally demonstrated that NCD/GaN substrates can outperform better than GaN (and Si) at elevated temperatures.

In chapter 6, we extend the study of thermal transport of advanced engineered materials from synthetic diamond into the realm of Bismuth Telluride-based thin film materials system. The chapter presents a comprehensive study of thermal conductivity in a new class of advanced material system – "pseudo-superlattices" of mechanically exfoliated Bi_2Te_3 thin film topological insulators (TIs). Experimental investigation on these stacked films shows an enhancement of up 250% in *ZT* figure of merit via reduction in the in-plane and cross-plane thermal conductivity with preserved electrical conductivity. Chapter 7 explores the thermal transport in another new advanced material – polycrystalline graphene (PCG) and graphene oxide (GOx) films. These films are getting much attention owing to their ability to be grown over large area and in mass quantities unlike the mechanically exfoliated graphene. Detailed study on thermal transport in these chemically grown large areas free standing films have been discussed. Result shows that although these films do not have thermal conductivity as high as single layer suspended graphene, but at the same time they can offer high thermal conductivity than copper thin films, and thus can find applications in interconnects, etc. The chapter presents a detailed study of thermal conductivity in these films, both free standing and substrate effect, thermal boundary resistance between PCG and Si interfaces, and specific heat capacity. Chapter 8 is devoted to the thermal conductivity enhancement in metallic

thermal interface materials (TIMs) with graphene as a filler material. It discusses the epoxy/graphene composite sample preparation and enhancement in thermal conductivity of TIMs with varying vol % of filler material – graphene experimentally. The experimental results have been compared with the theoretical predictions and the physical processes leading to the enhanced thermal properties have been elucidated. Conclusions are provided in chapter 9.

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Chapter 2

Thermal Engineering in Advance Materials and Devices

2.1 Introduction

Heat removal from integrated circuits is a critical issue for the electronics industry and limits miniaturization. Miniaturization combines with placing more channels within a unit volume of the device or circuits and dense packaging. As a result, more power needs to be dissipated as heat within a unit volume. To prevent devices and circuits from overheating and eventual breakdown, efficient heat removal techniques are necessary. Recent breakthrough in transistor technology by introduction of other new materials like germanium, silicides, and other dielectrics continue to add new thermal challenges. Placing near conductive and interconnect channels the components made of materials with high thermal conductivities allows to increase the rate at which the heat can be transferred away from the devices and circuits. On the other hand materials with very low thermal conductivity are the focus of recent quest for high-efficiency thermoelectric materials. So, materials with both very high and very low thermal conductivities are technologically important. For this reason, it is important to investigate thermal properties of materials at nanometer scale and identify materials with the extremely large or extremely low thermal conductivity for applications as heat spreaders or heat

insulators. Carbon has attracted much attention owing to its uniquely wide range of thermal conductivity. The various allotropes of carbon and their derivatives cover a wide range of thermal conductivity values from as low as 0.1 W/mK in diamond like carbon (DLC) [1] to above 5000 W/mK in single layer graphene [2-3]. Most of the heat in carbon materials is carried by lattice vibrations, i.e. acoustic phonons. The thermal conductivity of carbon materials depends on the structural disorder, sp3 or sp2 content of the material system, thickness and grain size of the films, and also on the dimentionality of the material system [4].

2.2 Advanced Engineered Materials: Thin Films and Superlattices

Size dependence of the thermal conductivity in thin metal films was first reported in mid-1960s [5-6]. Thin films are thin material layers ranging from fractions of a nanometer to several micrometers in thickness. The thermal conductivity of thin films have drawn increasing attention as it is a very important parameter to determine performance, reliability and device design of microelectronic devices, micromachined transistors, photonic devices, solid-state lasers, sensors, thermoelectric devices, and thermal barrier coatings [7-8]. Integrated circuits (ICs) employ various insulating, semiconducting and metallic thin films. Thin films used in microelectronics and photonic devices need to have high thermal conductivity in order to dissipate heat efficiently. On the other hand,

thermoelectric devices call for materials/structures with low thermal conductivity. The performance of thermoelectric materials is given by the figure of merit

$$ZT = S^2 \sigma T / K \qquad [2.1]$$

where S is the Seebeck coefficient, σ is electrical conductivity, T is the absolute temperature, and K is the thermal conductivity [9].

Metallic thin films are widely used in microelectronics and micromachined sensors and actuators. In metals, most of the heat is carried by electrons, phonon contribution is very small. Electron scattering at the thin film boundaries impose an additional resistance on the electron transport and thus size effects on thermal conductivity is observed [10-11]. Dielectric thin films serve as electrical insulators, optical coatings and thermal barrier coatings and this have wide applications in microelectronics, semiconductor lasers, and optical devices. Knowledge of thermal conduction in these films is essential for the reliability and performance of these devices [7-8]. In semiconductors the electron contribution to heat conduction is very small depending on the doping concentration. Several groups have done rigorous study of thermal conductivity of silicon thin films in the forms of single-crystalline, polycrystalline, and amorphous states [12-14]. These silicon films are important for silicon-on-insulator (SOI) ICs, sensors, actuators, etc. For polycrystalline and single-crystalline films, thermal conductivity is dramatically reduced compared to their bulk values due to phonon and electron scattering at boundaries, grain boundaries and

interfaces. For amorphous films, the microstructures, mass density and stoichiometry plays more significant role in thermal conductivity.

Superlattices, periodic structure of stacked layers of alternating two (or more) materials, have drastically reduced thermal conductivity in comparison to the corresponding bulk values, making them promising candidates for high-efficiency thermoelectric materials [15-17] and optoelectronic devices such as quantum well lasers and detectors [18]. Superlattices do not have to be composed of only two different materials, and the alternate layers do not need to be of same thickness. Chen *et al*. found that superlattice is anisotropic, with different thermal conductivity along in-plane and cross-plane directions [19]. The experiments and theories for these two directions are very different. Thermal conductivity in in-plane direction is not same to the corresponding bulk value, but it rather decreases owing to imperfect interface boundaries [20]. Cross-plane thermal conductivity of a superlattice is even lowered due to the thermal boundary resistance [21] between the layers and can further be decreased by intentionally introducing some degree of randomness in the layer thickness. This randomness induces Anderson localization of the phonons [22]. If the layers of superlattice are thick, all the heat is carried by phonons and Kapitza resistances at interfaces and Boltzmann equations for the interior of layers are sufficient to calculate thermal conductivity. When the layers are of nanometer thickness, one have to include the wave interference and nonlocal temperature scales [23-24].

Phonon-boundary and phonon-interfaces scattering emerges as the film thickness approaches the phonon mean-free-path (MFP) imposing additional resistance to the thermal transport. The complexity of structures, stoichiometry, boundary scattering, scattering at interfaces and imperfections in thin films and superlattices impose challenges to understand thermal transport in these advanced engineered materials. The existing models explaining thermal properties in thin films and superlattices are still not totally satisfactory.

2.2.1 Ultrananocrystalline and Microcrystalline Diamond

Bulk crystal diamond has the highest thermal conductivity among bulk solids, which at RT varies between 1000 – 2200 W/mK depending on its quality [25]. Recently, it was discovered that polycrystalline diamond films can be grown to obtain variable crystallite size, ranging from micrometer to few nanometers [26]. More recently, there has been growing interest to nanocrystalline diamond (NCD) which can be synthesized at rather low temperature through the argon-rich microwave plasma-assisted chemical vapor deposition process (MPCVD) as compared to the hydrogen-rich atmosphere required for microcrystalline diamond (MCD) [27]. These films, also known as ultrananocrystalline diamond (UNCD) are very smooth and free of pin-hole as compared to MCD. In UNCD, the sp^3 phase is ordered inside the grains and has a predominant clustering of sp^2 phase at the grain boundaries [27-28] where as MCD have predominant sp^3 phase owing to larger grain size. These polycrystalline diamond films have the potential to improve thermal

management in the electronic microstructures [7, 29]. However, not much is known about thermal conduction in these material systems.

The experiments results discussed in chapter 4 reveals that the effective thermal conductivity of synthetic diamond/Si composite substrates can outperform that of Si at elevated temperatures characteristic of current state-of-the-art devices. Experimental studies also explain strong dependence of thermal conductivity of polycrystalline diamond films on their grain size, film thickness, lattice imperfection and impurities, and interface quality. Grain boundaries play important role in phonon transport, which are strongly scattered at the grain boundaries. The grain size, grain geometry and other parameters can be controlled by varying the process condition and stoichiometry. This makes UNCD and MCD of significant importance in thermal engineering of microdevices as they can be tuned to provide both thermally conductive and insulating interfaces [30].

2.2.2 Graphene and Polycrystalline Graphene

Graphite has been known to have one of the highest thermal conductivity ~2000 W/mK in in-plane direction amongst carbon based materials [31]. After discovery of carbon nanotubes (CNT), one-dimensional form of carbon [32], several research groups reported very high thermal conductivity in CNTs, higher than those of graphite [33-34]. Measured thermal conductivity of an isolated multi walled CNT (MWCNT) were reported to be ~

3000 W/mK around RT [35]. Berber *et al.* [36] theoretically reported a very high value of ~6600 W/m K using molecular dynamic simulations. More recently, Andre Geim and Konstantin Novoselov discovered graphene - a single isolated layer of sp^2 hybridized carbon atoms arranged in a honeycomb lattice, for which they split the 2010 Nobel Prize in Physics [37-40]. Graphene was first isolated by micromechanical cleavage of bulk graphite [37] and exhibits a bunch of unique electrical and thermal properties [37, 2-3]. Balandin *et al*. [2] used a Raman spectroscopy based technique to measure the thermal conductivity of this truly two dimensional system - graphene, and reported thermal conductivity values ~ 5000 W/mK which are on the higher end of that reported for CNTs. Graphene's unique properties make it a realistic candidate for a number of electronic applications. One major problem is that the micromechanically cleavage technique allows only minute quantities of graphene which may be sufficient for fundamental research but is unlikely to become commercially viable. There has been rapid progress in alternative routes to produce large area graphene which includes chemical vapor deposition [41-42], epitaxial growth of graphene on electrically insulating substrates [43], reduction of graphene derivatives such as graphene oxide [44-45]. These films are not single crystal graphene and do not have thermal conductivity as high as single layer suspended graphene, but at the same time, they are much easier for synthesis in mass quantities and may find commercial applications.

Chapter 6 is dedicated to the experimental results on polycrystalline graphene (PCG) films and graphene oxide (GOx) films provided by Andre Geim's group, University of Manchester, U.K. The preparation method of these films has been reported

by Blake *et al* [46]. In order to measure thermal conductivity of the suspended films, the same technique as the one developed for suspended single-layer graphene was used [2-3]. Experiment and simulation results were combined to verify the thermal conductivity of PCG and GO films. The results discussed in chapter 5 reveals, that although these films have lower thermal conductivity as compared to that of pristine graphene, they can outperform thermal conductivity of copper thin films and may find applications in interconnects, etc. The thermal conductivity in these films is dependent on the individual graphene flakes as well as the density of the flakes, and hence can be tuned by further refining the preparation technique.

2.2.3 Stacked Bi_2Te_3 Thin Film "Pseudo-Superlattices"

Bismuth telluride (Bi_2Te_3), a narrow band gap semiconductor, is the best known candidate for thermoelectric applications owing to its highest thermoelectric figure of merit, ZT~1 at room temperature (RT). Recently it was discovered that Bi_2Te_3 family of materials are topological insulators (TIs). TIs are materials with a bulk insulating gap and conducting surface states that are topologically protected against scattering by the time-reversal symmetry. It was shown theoretically that ZT can be strongly enhanced in Bi_2Te_3 thin-film TIs provided that the Fermi level is tuned to ensure the surface transport regime and the films are thin enough to open a gap in the "Dirac cone" dispersion on the surface [47-48]. We used our expertise on "graphene-like" process for exfoliating Bi_2Te_3 films. We have recently demonstrated a "graphene-like" mechanical exfoliation of the

atomically-thin single-crystal films and ribbons of Bi_2Te_3 [49]. Any practical application of thermoelectric nanostructures requires a sufficient bulk volume. With this motivation, we designed and fabricated "*pseudo-superlattices*" by stacking of mechanically exfoliated single-crystal Bi_2Te_3 films and experimentally investigated their thermoelectric properties [50].

Chapter 7 summarizes the experimental results on mechanically exfoliated stacks of thin films of Bi_2Te_3 and reveals that *ZT* in such structures can be substantially increased via reduction of the in-plane as well as cross-plane thermal conductivity. Strong decrease in the thermal conductivity with preserved electrical properties translates to ~140-250% increase in *ZT* at RT. It is suggested that the film thinning to *few-quintuples* and tuning of the Fermi level can help in achieving the topological-insulator surface transport regime with an extraordinary thermoelectric efficiency.

2.3 Thermal Interface Materials

There is a call for improved thermal interface metarials (TIMs) which facilitate heat transfer across interface by reducing the contact resistance between the heat-generating chip and heat-sinking units. The selection of a suitable TIM material to fill the interface between a chip and a heat spreader is critical to the performance and reliability of the semiconductor device. Recently, there has been a transition from polymer based TIMs to the ones with metallic particles and spheres as fillers to cope up with the demand of increased thermal conductivity. The thermal conductivity enhancement by loading of the

metal particles is limited by their thermal contact with each other and with the surfaces across which the TIM is applied [51]. The needs for improved thermal interface materials (TIMs) in modern electronic chip packaging and high-power density photonic devices stimulated interest to carbon materials as fillers for TIMs. Current TIMs are based on polymers or greases filled with thermally conductive particles such as silver or silica, which require high volume fractions of filler (up to ~70%) to achieve thermal conductivity of about 1-5 W/mK of the composite. Carbon materials, which were recently studied as fillers include carbon nanotubes (CNTs), graphite nanoplatelets (GNPs), graphene oxide nanoparticles (GONs), and graphene flakes derived by chemical processes. The studies mentioned difficulties in achieving high filling ratios of CNTs and their aligning. In addition, the cost of CNTs continues to be too high for industrial applications.

Chapter 8 is dedicated to the experimental results on thermal conductivity in TIMs with metallic fillers as well as graphene fillers simultaneously. A number of disk-shaped samples were prepared by dispersion (via high-shear mixing) of aqueous graphene solution in to the silver epoxy paste (metallic TIM) followed by thermal treatment to remove remaining solvent and air bubbles from the silver epoxy/graphene composites. Chapter 8 reveals the data of thermal conductivity studies done on several epoxy/graphene specimens which were prepared with varying graphene loading from 0.5 to 3 weight % and elucidate the physical phenomena of enhancement in thermal conductivity of metallic TIMs with graphene fillers.

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Chapter 3

Experimental Methodology

3.1 Introduction

In this chapter, the experimental methodology to study the thermal transport in advanced engineered materials is described. A complete theoretical background of the experimental technique has been provided. The chapter discusses the method of sample preparation for the experimental measurements and also describes the experimental setup. Several practical considerations, from sample size requirement to the elimination of thermal contact resistance, will also be discussed.

3.2 Transient Plane Source (TPS) "Hot Disk" Thermal Conductivity Measurement Technique

Hot Disk is a transient technique for thermal studies on various sample types was first proposed by Gustaffson [1]. Hot Disk is designed to non-destructively measure thermal conductivity and thermal diffusivity of solid, fluid and powder materials as well as materials with anisotropic thermal properties. The thermal transport properties of solids vary extensively depending on the structure, pressure, temperature, density, etc., of different materials. The main motive behind the development of the TPS technique has

been to include large ranges of the transport properties and also to apply the same technique to large variety of materials [2]. The Hot Disk Thermal Constants Analyzer can be used for measuring thermal properties of a large variety of materials with thermal conductivities ranging from 0.005 W/mK to 500 W/mK over a wide temperature range.

The prime component in the Hot Disk system is the sensor (probe). The most compact and convenient sensor for measurements is the plane one, comprising a bifilar spiral. With this design the area of the sensor is minimized while the electrical resistance can be made comparatively large. The Hot Disk sensor probe comprises a flat resistive element with a continuous double-spiral of electrically-conducting nickel (Ni) metal etched out of thin foil and sandwiched between two layers of Kapton to provide both electrical insulation from the sample and mechanical stability for the sensor. The Nickel foil is chosen because of its high and well-known temperature coefficient of resistivity (TCR). This coil has a temperature coefficient (TCR) which can be deduced accurately for resistance recording. This nickel spiral is supported on both sides with a thin electrically insulating material. In TPS method, this electrically insulated flat nickel sensor plays a role of the heater and thermometer simultaneously. It is placed between two pieces of a sample under investigation. During the experiment, a constant current pulse is passed through the sensor, which generates heat. The heat generated dissipates through the sample on either side at a rate dependent on the thermal transport properties of the surrounding material. The temperature increase in the sensor is accurately determined through resistance measurement. Thermal properties of the material can be

accurately determined by recording temperature rise as a function of time in the sensor. Figure 3.1 shows the nickel bifilar sensor.

Nickel metal can be used as a sensor material over a large temperature range. In experiments performed with the Hot Disk, it can be used from 250K to 700K. However, it is not possible to use the same insulating material to support the Nickel spiral throughout this temperature range. From cryogenic temperatures to about 500K thin Kaptan films with a thickness of 12.7μm or 25μm, is being used. This gives a total thickness of the sensor between 60μm and 80μm. For measurements from 500K to 1000K Mica insulation, with a thickness of around 0.1mm, is being used, making the total thickness of the sensor about 0.25mm. To accommodate a broad range of materials and sample sizes, a wide selection of sensor sizes is available.

Figure 3.1: TPS nickel bifilar sensor with kapton insulation. Nano-Device Laboratory, UCR.

3.3 Theory of the Hot Disk Technique

Hot Disk utilizes a bi spiral sensor element between two pieces of the sample being tested. During a transient recording the sensor is electrically heated (from 0.5 K to 5 K)

and at the same time the resistance or the temperature increase of the Nickel double spiral is monitored. The heat generated in the sensor is dissipating in all directions into the surrounding two sample pieces. During a pre-set time, 200 resistance recordings are taken and from these the relation between temperature and time is established. In order to obtain a reasonably higher initial resistance of the sensor element, the Hot Disk sensor has been designed in the form of a double spiral in order to minimize the total size of the sensor as well as to make it work with a convenient and compact configuration of the sample.

In the theoretical treatment, a hot disk sensor can be approximated as a sensor with *m* number of concentric rings which are equally spaced, since the sensor is designed to have uniform power density throughout the disk. Let *a* is the radius of largest ring, then the radius of smallest ring is *a/m*. Then, the total length of the heating filament is

$$L = \sum_{l=1}^{m} 2\pi l \frac{a}{m} = (m+1)\pi a \qquad [3.1]$$

Starting from the equation of heat conduction and its instantaneous point source solution, the mathematical expression of the temperature increase in the sensor surface can be obtained by integrating the point source solution over the source volume and time. During a hot disk measurement, we can only measure the temperature increase for the sensor itself. Thus, we need to determine the average temperature increase for the sensor only. This can be done by averaging the temperature rise of ring source over the length of the concentric rings. This final time dependent temperature increase [3, 4] is given by

$$\overline{\Delta T(\tau)} = \frac{P_0}{\pi^{3/2} aK} D(\tau) \qquad [3.2]$$

Where P_0 is the total power output from the sensor, *a,* the radius of the sensor disk, *K* is the thermal conductivity of the sample that is being tested and $D(\tau)$ is a dimensionless time dependent function given by

$$D(\tau) = [m(m+1)]^{-2} \int_0^r \sigma^{-2} d\sigma \left[\sum_{i=1}^{m} l \sum_{k=1}^{m} k \exp\left\{ \frac{-(l^2+k^2)}{4m^2\sigma^2} \right\} I_0\left\{ \frac{lk}{2m^2\sigma^2} \right\} \right] \qquad [3.3]$$

Eq. 3.2 shows that the average temperature increase in the hot disk sensor is proportional to function $D(\tau)$ which is a rather complicated function of dimensionless parameter $\tau = \sqrt{kt}/a$, where k is the thermal diffusivity, t is the transient measurement time. The expression given by eq 3.2 which directly relates the temperature increase in the sensor surface to the sensor configuration, the output power, and the transport properties of the surrounding material, forms the basis of the hot disk measurement. $D(\tau)$ can be accurately evaluated to five or six significant figures if the dimensions of the sensor are known. The average temperature increase across the hot disk sensor area can be measured by monitoring the total resistance of the hot disk sensor

$$R(t) = R_0 \left[1 + \alpha \overline{\Delta T(\tau)} \right] \qquad [3.4]$$

where $R(t)$ is the total resistance at time *t*, R_0 is the resistance of the TPS/sensor element before the transient measurement starts, α is the temperature coefficient of the resistance (TCR) of the TPS element, which is well known for nickel. Thus, this expression allows us to accurately determining $\overline{\Delta T(\tau)}$.

If the relation between *t* and τ is known, ΔT can be plotted as a function of $D(\tau)$, and a straight line should be obtained with slope equal to $P_0 / \pi^{3/2} aK$, from which thermal conductivity, *K* can be calculated. Now τ depends on thermal diffusivity *k*, which is unknown. To calculate the thermal conductivity accurately, a series of computational plots of ΔT versus $D(\tau)$ are plotted for a range of *k* values, to get a final straight line once experiment is completed. This iteration process is can be done by software by optimizing output power of the sensor and the measurement time until an optimized value of *k* is found. Therefore, both thermal conductivity and thermal diffusivity of the sample can be obtained by recording the single transient measurement using a hot disk sensor.

3.4 Experimental Setup for the Hot Disk Measurements

The experiments with the hot disk are performed with the sensor sandwiched between two thin samples of equal thickness. The sensor works both as temperature sensor and heat source. The thermal conductivity equation has been solved to show the theoretical time dependence of the temperature increase; but if the transient recording is extended for a longer period for a one-dimensional sample, the temperature versus time graph becomes a straight line [5] which indicates stabilization. Such experimental conditions give values of specific heat capacity. In slab method the sensor is sandwiched between two thin circular slabs of the sample, making arrangements such that it can be assumed that the slabs are thermally insulated, so that the total input power is much more than the heat dissipation at the boundary (requirement for transient recording). This experimental

method is intended for studies of the thermal conductivity and thermal diffusivity of medium- or high conducting materials (Usually with thermal conductivity greater than 10 W/mK). This method is very similar to the standard method. The two differences between the two methods are, first, the outside lateral surfaces of the sample slabs need to be insulated by a material with low thermal conductivity in order to reduce the heat losses to the surroundings. Second, heat propagates mainly in the direction of the slab plane and it is assumed that the sample is infinite in this plane. This method is also good for ceramics, metals, silicon wafer, thin films etc. Figure 3.1 shows the schematic of sensor-sample setup where sensor is sandwiched between two pieces of sample and acts both as heat source and thermometer.

The sample thickness t, and sensor radius a, should obey the relation $0.03 < (t/a) < 0.75$. The choice of sensor radii to match different samples is thus critical. When the transient recording begins, initially the probing depth $\Delta p < (r\text{-}a)$ where r, radius of the sample and a, radius of the sensor. The heat pulse has not yet reached the first surface of the sample; and under this condition, the thermal conductivity of the sample is evaluated. The temperature increase is expressed in terms of the characteristic time of the hot disk as in equations (3.2). When the time,

$$t \geq C_{r-a} \qquad [3.5]$$

where $C_{r-a} = (r-a)^2 / k$; a constant temperature gradient is established all through the sample. In this case, $(r-a)$ is considered to be the largest distance from the sensor to the lateral sample boundary, if the geometry is non-symmetrical. The temperature increase in the sensor will then be denoted by

$$\overline{\Delta T(t)} = K + \frac{Pt}{C_p M} \qquad [3.6]$$

Here P is output power, M is the mass of the sample, C_p is the specific heat per unit mass. This is a linear function of t. Having known the specific heat per unit volume (ρC_p), we can calculate the thermal diffusivity, k from the equation $K = k\rho C_p$

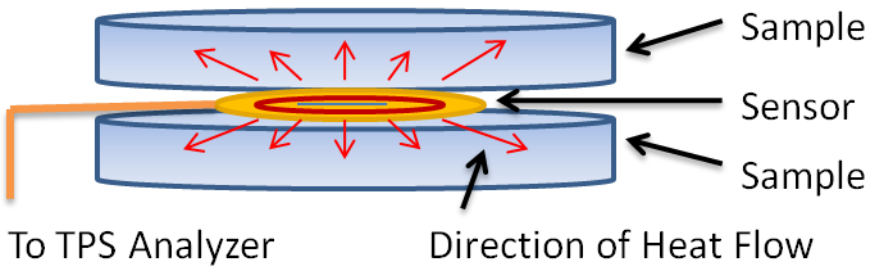

Figure 3.2: Schematic of sensor-sample set-up in TPS hot disk technique. Reprinted with permission from V. Goyal, S. Subrina, D. Nika, and A.A. Balandin, "Reduced Thermal Resistance of the Silicon - Synthetic Diamond Composite Substrates at Elevated Temperatures," *Appl. Phys. Lett*., vol. 97, 031904, 2010 © 2010 American Institute of Physics.

The Hot Disk TPS instrument is coupled with the HAAKE hot bath and VECSTAR hot furnace for the temperature dependent measurements. Figure 3.3 shows the pictures of hot bath and hot furnace. The measurement needs to be performed at isothermal conditions and hence some settling time (45 sec/50 sec) is given to the metal holder- sample set up in the hot bath or furnace. The thermal response of the bath/furnace and the metal holder damps out the temperature fluctuations inside and maintains a sensitivity of about 1%. For temperature stability of ± 0.1ºC, the bath liquid should allow

a good circulation and minimize heating in pump. To meet this criterion, a mixture of ethylene alcohol 50% and water 50% has been used as the circulating fluid and its operating range is -20ºC to 100ºC in hot bath. With hot furnace thermal conductivity measurements can be done from 25ºC to 500ºC depending on the insulation material of the sensor.

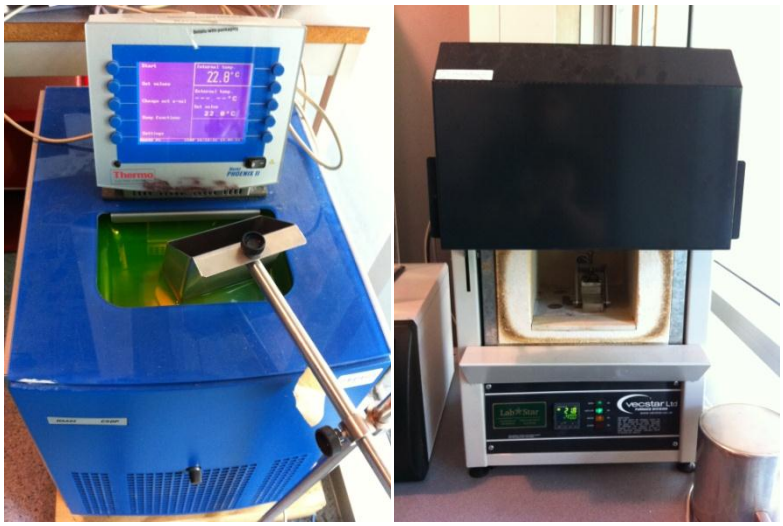

Figure 3.3: Picture of hot bath and the hot furnace coupled with TPS hot disk technique for temperature dependent thermal conductivity measurements. Nano-Device Laboratory, UCR.

3.5 Hot Disk Measurement Procedure and Practical Considerations

The thermal conductivity equation derived above is based on the assumption that the sensor is located in an infinite material. This entails that the total time of the transient recording is limited by the presence of the outside boundaries of the sample. The shortest

distance from the sensor to the outside sample surface defines the available probing depth, and should never be less than the radius of the sensor. This actually indicates how far the heating pulse has propagated into the sample during the time period *t*. It has been shown analytically that if the probing depth is

$$\Delta p \geq \sqrt{4kt} \qquad [3.7]$$

then the influence of the sample size on the final result will be negligible [6]. This gives an estimate of the sample size and the maximum time of the transient recording. The length of the current pulse is normally chosen short enough so that the TPS element can be considered in contact with an infinite or semi-infinite solid throughout the transient recording. This means that the time of a transient recording must be chosen so that the outer boundaries of the sample do not influence the temperature increase of the element to any measurable extent.

Another practical issue is the interfacial thermal resistance between the sample surface and the sensor. In hot disk technique, the sensor insulating layers (Kapton or mica) adds an additional contact resistance. However, it was estimated that the influence of contact resistance on the average temperature increase becomes a constant, ΔT, after a short period of time [6, 7]

$$\overline{\Delta T(\tau_c)} = \Delta T + \frac{P_0}{\pi^{3/2} aK} D(\tau_c) \qquad [3.8]$$

where ΔT is inversely proportional to the thermal conductivity of the insulating layer and is related to the dimensions of the insulating layer. This time can be estimated as

$$\Delta t_i = \delta^2 / k_i \qquad [3.9]$$

where δ is the thickness of the insulation layer and k_i is the thermal diffusivity of the insulation material [8]. Numerical simulations have shown that for a 25μm thick Kapton insulation layer the time needed for ΔT to become a constant is typically ~50ms [9]. Thus, this term can be easily separated in the software when $\overline{\Delta T(\tau)}$ is plotted versus $D(\tau)$ using the data points generated after t > 50ms.

3.6 Summary

In summary, theory of the hot disk technique for thermal conductivity measurement was discussed from the first principles. The hot disk sensor, composed of a double spiral nickel wire, is approximated as *m* concentric rings. The sensor is used as a heat source as well as a temperature monitor. During the thermal conductivity measurement, the sensor is sandwiched between two halves of the sample; a constant current is supplied to the sensor. During the measurement, the sensor temperature as a function of time t or characteristic time τ has a strong dependence on the thermal transport properties of the surrounding material. Starting from the point source solution for thermal conduction is an infinite isotropic substance, the average temperature increase ΔT near the sensor surface is obtained as a function of τ. ΔT is proportional to a complicated function *D(τ)* which can be calculated numerically if the sensor configuration is known. When proper τ value

is chosen based on optimization as described above, the slope of $\overline{\Delta T(\tau)}$ versus $D(\tau)$ is inversely proportional to thermal conductivity of the sample. As a special case, the thermal conductivity measurement of thin slab samples can be performed by insulating the outer surfaces of the sample. Theoretically, the conduction problem can be solved by introducing the image sources, and a modified function $D_s(\tau)$ can be obtained [3]. Again, the slope of $\overline{\Delta T(\tau)}$ versus $D_s(\tau)$ is inversely proportional to thermal conductivity of the thin slab sample. With proper corrections, the hot disk technique provides an excellent tool for rapid and accurate measurement for both thermal conductivity and thermal diffusivity of a wide range of materials. This technique is capable of measuring the thermal conductivity over a wide range of temperature with high accuracy. The hot disk technique is a valuable tool for material inspection and selection

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Chapter 4

Thermal Conductivity of Ultrananocrystalline and Microcrystalline Diamond Thin Films

4.1 Introduction

A wide variety of the carbon-based materials, including diamond, diamond-like carbon (DLC), carbon nanotubes (CNT) and graphene [1] have recently attracted attention as possible candidates for the prospects of hybrid Si – carbon electronics*. Diamond has been attracting attention as a potential material for heat management in electronics [2]-[5]. The thermal conductivity of natural diamond is very high and exceeds the thermal conductivities of either aluminum, copper, or, even, silver [6], the materials that can be used for interconnects. The thermal conductivities of semiconductor materials used in transistors are also lower to that of natural diamond. In addition to its record high thermal conductivity, diamond has a number of other exceptional properties such as tremendous hardness, chemical inertness, high mobility of charge carriers and high electron emission at low fields [7-8].

*Part of this chapter has been excerpted from V. Goyal, S. Subrina, D. Nika, and A.A. Balandin, "Reduced Thermal Resistance of the Silicon - Synthetic Diamond Composite Substrates at Elevated Temperatures," *Appl. Phys. Lett.* vol. 97, 031904, 2010. © 2010 American Institute of Physics.

At the same point, it is rather unrealistic to successfully apply natural diamond in manufacturing electronics. Thus techniques to fabricate polycrystalline diamond components were developed and are currently used by industry. The processes to fabricate diamond components for semiconductor devices and circuits use primarily Chemical Vapor Deposition (CVD) techniques. There is a variety of methods to produce synthetic polycrystalline diamond, but most of the CVD processes use mixtures of methane (as carbon precursor), hydrogen and argon under high temperatures and pressures. Using the CVD, one can produce polycrystalline diamond (or synthetic diamond) with specific grain sizes, material properties, hardness, surface roughness, etc., by varying mass ratios of three above mentioned gases, the temperature and the pressure in the reactor, the temperature of the substrate and other parameters. Table 4.1 lists some of the properties of different polycrystalline diamond films available: MCD, UNCD and NCD films. The UNCD films which are synthesized by the argon-rich microwave plasma assisted chemical vapor deposition (MPCVD) process, can have the grain diameter as small as d~2-5 nm.

Most recently, there was a notable increase in interest to composite silicon – synthetic diamond (Si-Di) substrates as alternatives to conventional silicon (Si) wafers. It is driven by several factors. First, continuing downscaling of Si complementary metal-oxide semiconductor (CMOS) technology demands more efficient heat removal to handle the increasing thermal design power and rising temperature (T) of hot spots [9-11]. The high T in the transistor channels translates into degraded mobility, μ, and, as a result, leads to smaller speed and drive current. Second, there was a renewed interest to Si-Di

substrates owing to fast progress in the chemical vapor deposition (CVD) of ultrananocrystalline diamond (UNCD) and microcrsyatlline diamond (MCD) [12].

Table 4.1: Properties of CVD grown polycrystalline diamond films.

Film Type	*MCD*	*NCD*	*UNCD*
Grain size	> 1 µm	10 - 1000 nm	< 10 nm
Surface Roughness	10-25% of thickness	Typically < 100 nm	Typically < 20 nm
Relative Hardness	100%	95%	90%
Friction Coefficient	High unless polished	Moderate – may require polishing	Low but ambient dependant
Transparency	Medium to High	Low	Very Low
Thermal Conductivity	Medium to High	Low	Very Low
Process Window	Broad	Narrow	Very Narrow
1330 Raman Peak	Visible	Very Low	Not Visible

Conventional CVD film deposition methods employ microwave plasma-enhanced CVD or hot filament CVD with hydrogen rich chemistry (H_2:CH_4=0.1:4%). MCD films exhibit a columnar grain structure whose grain coarse with thickness, thus they exhibit a rough, highly faceted morphology. On the other hand, UNCD is grown using an Ar-rich/CH_4 chemistry in a microwave plasma-enhanced CVD process (Ar:CH_4=99:1%) [12]. It has also been demonstrated that UNCD films can be synthesized at temperatures that CMOS devices can withstand [13]. Additional motivations for Si-Di substrates include rising cost of Si because of growing demand for photovoltaic applications, prospects of hybrid Si – carbon electronics, which would include different allotropes of carbon, e.g. diamond, diamond-like carbon (DLC), carbon nanotubes (CNT) and graphene, as well as proposals for the *phonon-engineered* mobility enhancement in nanometer scale Si channels with diamond barriers [14-15].

At the same time, the heat conduction properties of synthetic diamond are not nearly as good as those of crystalline diamond. The thermal conductivity, *K*, of high-quality single-crystal diamond is ~2200 W/mK [16]. The room-temperature (RT) thermal conductivity of MCD is ~550 W/mK [17] while that of UNCD is much smaller than that of Si [18]. The "effective" thermal conductivity, K_{eff}, defined for the whole MCD/Si and UNCD/Si substrates, depends on the polycrystalline-diamond grain size, diamond layer thickness and interface quality. The surface roughness for MCD is usually much larger than that for UNCD. The rougher interfaces results in higher thermal boundary resistance (TBR), which offsets the thermal conductivity increase due to a lager grain size. Considering that RT thermal conductivity of Si is ~145W/mK it is not clear if

incorporation of synthetic diamond can improve the heat removal at the present state of technology for diamond deposition. For this reason, the conventional belief was that one has to wait for improvements in the CVD diamond until the composite Si-Di wafers can become practical for CMOS integration from the thermal management point of view.

In this chapter, we report the experimental study of the "effective" thermal conductivity, K_{eff}, of UNCD and MCD films on Si wafers using transient plane source 'hot disk' technique. To study the effect of the grain size and film thickness on thermal conductivity, some of the samples had approximately the same grain size, defined by the growth conditions, but different thicknesses while other samples had the same thickness but different grain sizes. The Si-Di samples used for the thermal conductivity study were rigorously characterized by the optical microscopy, scanning electron microscopy (SEM) and micro-Raman spectroscopy.

4.2 Sample Preparation and Characterization

For this study we used a set of samples with UNCD (Advanced Diamond Technologies) and MCD (sp3 Diamond Technologies) films grown on conventional 100 mm Si wafers in a microwave plasma CVD reactor. The UNCD/Si composite wafers were processed via CVD method using a gas composition CH_4:H_2:Ar = 1:1-5%:98-94% with 50 Torr deposition pressure and MCD/Si composite wafers were processed using gas composition CH_4:H_2 = 1 – 5% and Ar: H_2 = 0 – 95% with 100 Torr deposition pressure (sp3 Technologies, Model 650).

The surface morphology of the UNCD and MCD was characterized using the scanning electron microscopy (SEM). Film surface SEM images revealed that the average grain sizes for UNCD films were 5 – 10 nm (see Fig. 4.1) and the grain sizes for 0.91μm thick and 7μm thick microcrystalline diamond samples were 0.5-0.8μm and 1-3μm respectively (see Fig. 4.2 (a), (b)).

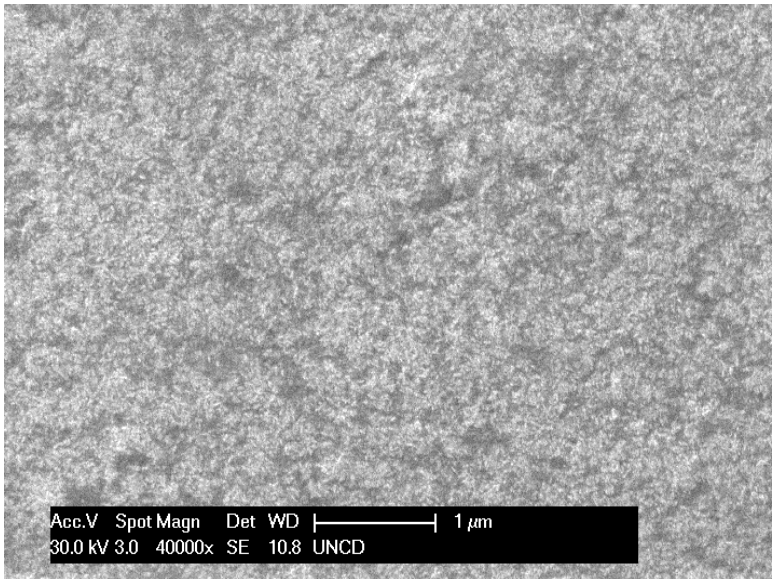


Figure 4.1: Top view SEM image revealing the grain sizes for UNCD films on Si. Reprinted with permission from V. Goyal, S. Subrina, D. Nika, and A.A. Balandin, "Reduced Thermal Resistance of the Silicon - Synthetic Diamond Composite Substrates at Elevated Temperatures," *Appl. Phys. Lett*. vol. 97, 031904, 2010. © 2010 American Institute of Physics.

To study the effect of the grain size and film thickness on thermal conductivity, some of the samples had approximately the same grain size, defined by the growth conditions, but different thicknesses while other samples had the same thickness but

different grain sizes. A sharp distinct interface between diamond and silicon was observed on each wafer via cross-sectional SEM (see Fig. 4.3 (a), (b)).

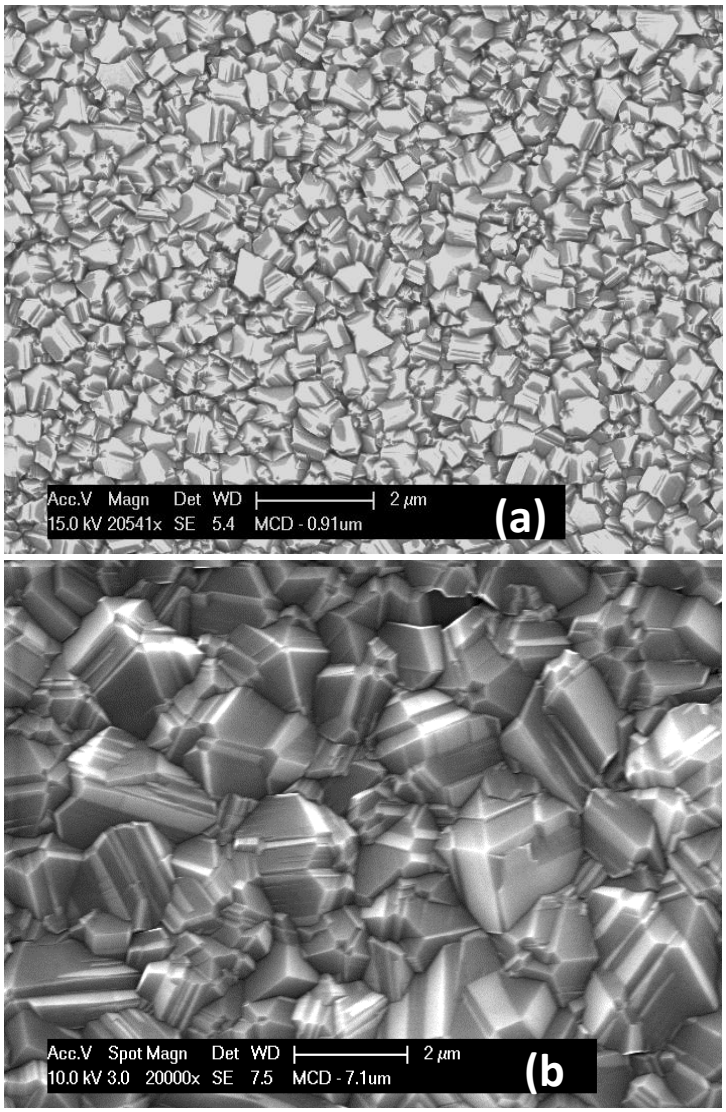


Figure 4.2: Top view SEM images of two MCD films with different grain sizes on Si. Reprinted with permission from V. Goyal, S. Subrina, D. Nika, and A.A. Balandin, "Reduced Thermal Resistance of the Silicon - Synthetic Diamond Composite Substrates at Elevated Temperatures," *Appl. Phys. Lett*. vol. 97, 031904, 2010. © 2010 American Institute of Physics.

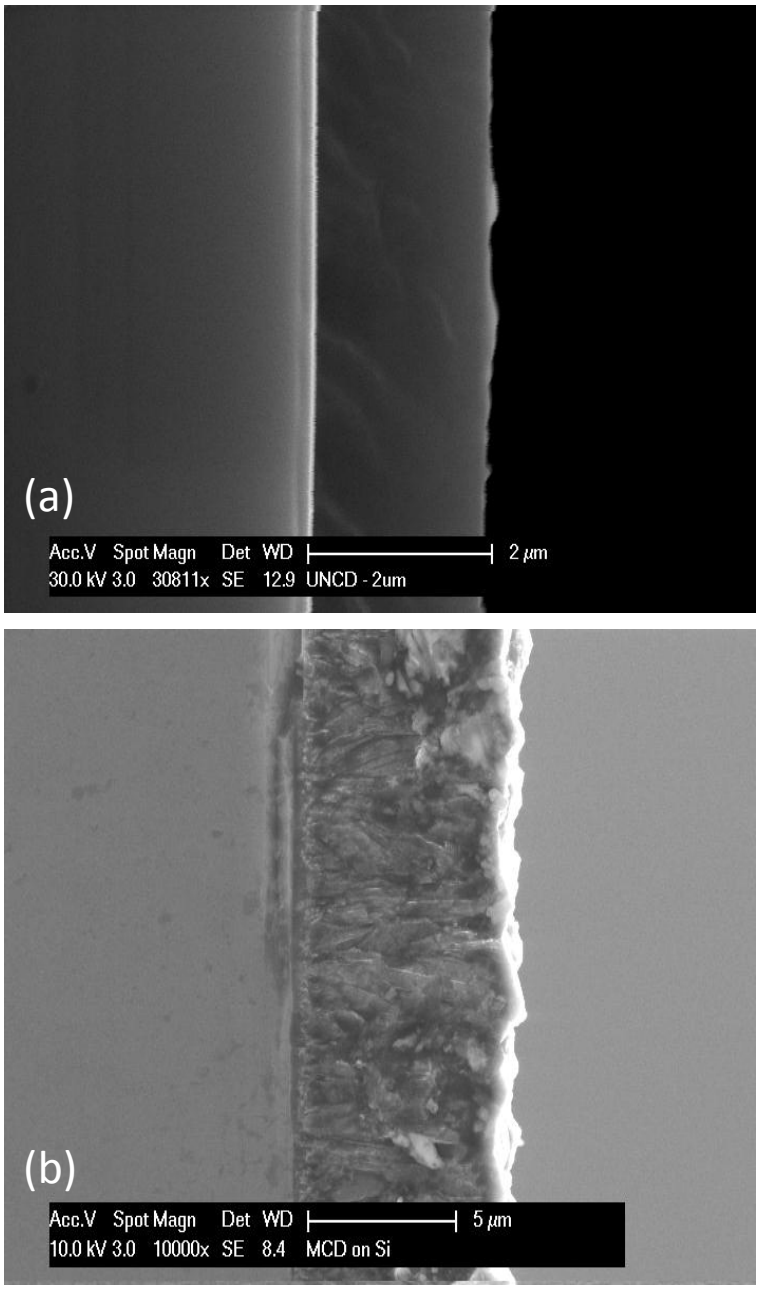


Figure 4.3: Cross-sectional SEM images of (a) UNCD/Si (b) MCD/Si interface. Reprinted with permission from V. Goyal, S. Subrina, D. Nika, and A.A. Balandin, "Reduced Thermal Resistance of the Silicon - Synthetic Diamond Composite Substrates at Elevated Temperatures," *Appl. Phys. Lett*. vol. 97, 031904, 2010. © 2010 American Institute of Physics.

For better characterization and identification of synthetic diamond films, Raman spectroscopy was carried out under 488-nm laser excitation. The Raman spectra for MCD and UNCD are qualitatively different. The 1332 cm^{-1} peak was absent in spectra of all UNCD films while being the most prominent feature in MCD films' spectra. Figure 4.4 (a) and (b) shows the Raman spectra of UNCD and MCD films respectively. The observed features were in line with reported data [17].

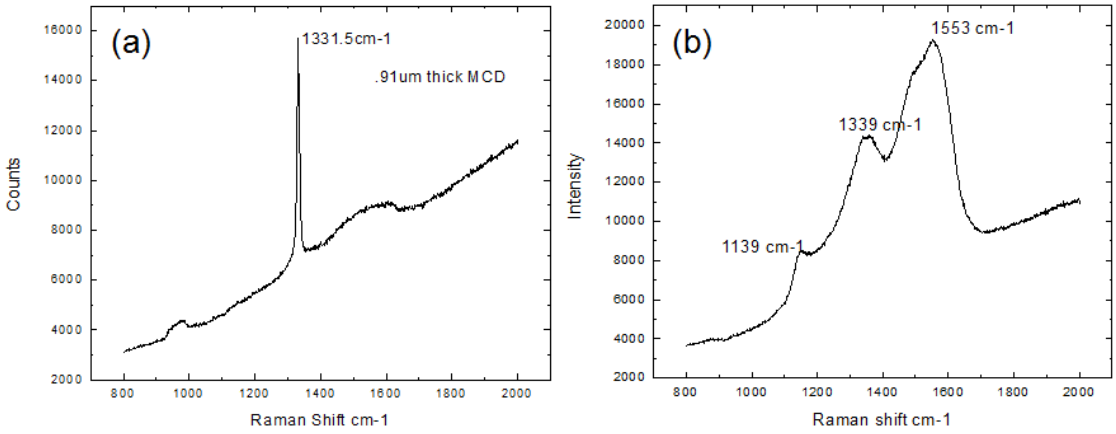


Figure 4.4: Raman spectrum of (a) MCD (b) UNCD films. There is a sharp 1330 peak for MCD films which is absent in UNCD films.

Along with the 1330 cm^{-1} peak, other peaks observed in the UNCD samples are 1140 cm^{-1}, overlapping peaks at 1450 cm^{-1} and 1560 cm^{-1}. The origin of 1140 cm^{-1} and 1450 cm^{-1} peaks is attributed to the sp^2 phase in the *trans*-polyacetylene segments at the grain boundaries [19, 20]. The peaks at ~1330 cm^{-1} and 1560 cm^{-1} are D and G bands, respectively associated with the sp^2-bonded carbon at the grain boundaries [13, 21]. It has

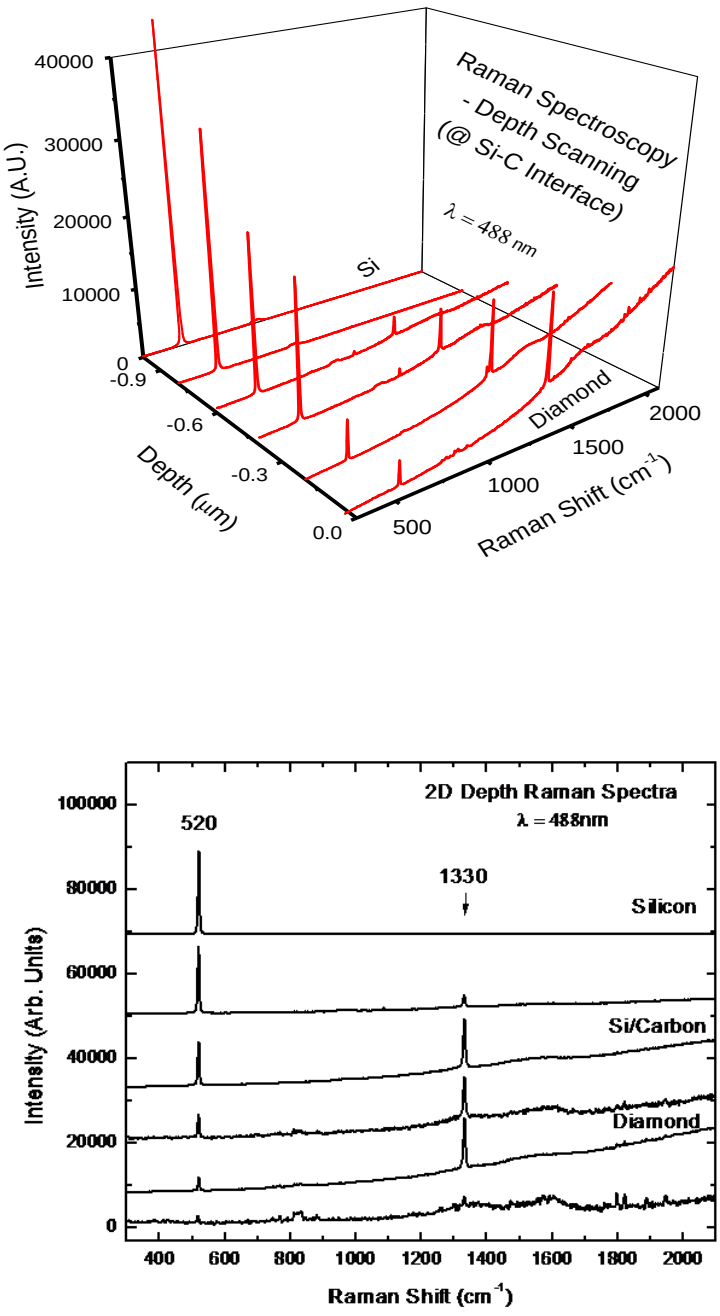


Figure 4.5: Series of Raman spectra found as the Si/Di samples scanned at different depth penetration to see if there is any SiC formation. Image is courtesy of Dr. Desalegne Teweldebrhan, Nano-Device Laboratory, UCR.

been noted that the broadening of the D band is due to the decreasing grain size from micro to nanometer scale [22].

Raman scans of Si/Di substrates were examined at several points in the cross section of the sample to check if there is any SiC formation between the diamond-silicon interfaces. By changing the confocal penetration depth of Raman laser we were able to differentiate and highlight relative Raman response of material in Si/diamond heterostructure. Microscopic transition from silicon substrate to that of first layer of diamond can be easily seen (see fig. 4.5(a)). A closer look at silicon-diamond interface shows that Si-Si bond peak decreases as one scan from Si wafer into diamond barrier layer. The diamond peak at 1330 cm^{-1} confirms the material quality. The absence of SiC peak suggests no formation of SiC. All these Raman scans reveals that the heterostructures have a good/smooth material interface.

4.3 Thermal Conductivity of UNCD/Si and MCD/Si Wafers

The thermal conductivity measurements on synthetic diamond/Si composite wafers were carried out using the transient plane source (TPS) technique referred as "hot-disk AB" [23, 24] which has already been "calibrated" with the 3-ω method [25, 26], which is considered to be a standard technique for thin films. Thermal conductivity measurements were performed for a wider temperature range of 20 ^{0}C to 250 ^{0}C with the help of coupled "hot furnace" with the "hot-disk AB" system. With the TPS technique, the probe comprises a flat sensor with a continuous double-spiral of electrically-conducting Nickel

(Ni) metal etched out of thin foil and sandwiched between two layers of Kapton which provides both electrical insulation from the sample and mechanical stability for the probe. The sensor is placed in-between the surfaces of two pieces of the sample to be investigated in such a way that the sensor makes a firm contact with both the pieces. During the measurement, a current is passed through the sensor which creates an increase in temperature. The heat generated dissipates through the sample on either side at a rate dependent on the thermal transport characteristics of the material. This sensor acts both as the heat source as well as thermometer to sense the temperature rise in the sample. Thermal properties of the material can accurately be calculated by recording the temperature versus time response in the sensor using the equation

$$\overline{\Delta T(\tau)} = P(\pi^{3/2} rK)^{-1} D(\tau) \qquad [4.1]$$

where τ is the parameter related to the thermal diffusivity α and the transient measurement time t_m through the expression $\tau = \left(t_m \alpha / r^2\right)^{1/2}$, r is the radius of the sensor, *P is* the input power for heating the sample, *D(τ)* is the modified Bessel function, and *K* is the thermal conductivity of the sample that is being tested. The time dependent temperature increase depends on such factors as the geometry of the sensor, the total power output, and the thermal diffusivity and the thermal conductivity of the sample. The time and the input power for the transient recording must be chosen so that the heat flow is within the sample boundaries and the temperature increase of the sensor is not influenced by the outer boundaries of the sample. According to TPS theory, to avoid any boundary influence, the sample is assumed to be infinitely large. Practically, the optimum ratio of sample size and sensor size is governed by the probing depth given by Δ_p =

$\beta(kt_{max})^{1/2}$, where t_{max} is the total time of the transient recording, k is the thermal diffusivity and β is the constant of the order of unity [23-24, 27]. The optimal transient measurement time needs to be selected within the interval $0.3 < t_m/\theta < 1.1$ provided $t_m < t_{max}$ [28]. To accommodate for optimum probing depth we chose 0.8 W and 0.5 W as input power pulse for duration of 4s for MCD/Si substrates and reference Si samples using 6.403 mm radius disk shaped sensor.

Figure 4.6 represents typical plot of the temperature rise in TPS measurements for MCD/Si substrates, as well as the temperature rise in the reference Si sample. The larger temperature rise for MCD/Si films illustrates the difference in thermal resistance between these composite substrates with respect to Si. Figure 4.7 shows the schematic of sensor sandwiched between two sample pieces during the experiment. Sensor with radius 6.40 mm was used for the measurements. By making the computational plot of the recorded temperature increase versus time, we get a straight line, the intercept of which is ΔT and the slope is $P/\pi^{3/2}rK$. The thermal diffusivity, k is obtained through iteration process. Thereafter, thermal conductivity can be calculated after we get final straight line once experiment is completed. For all our measurements, total to characteristic time ratio, t_m/θ was ~6.38 to 7.5 which confirms the reliability of our measurements.

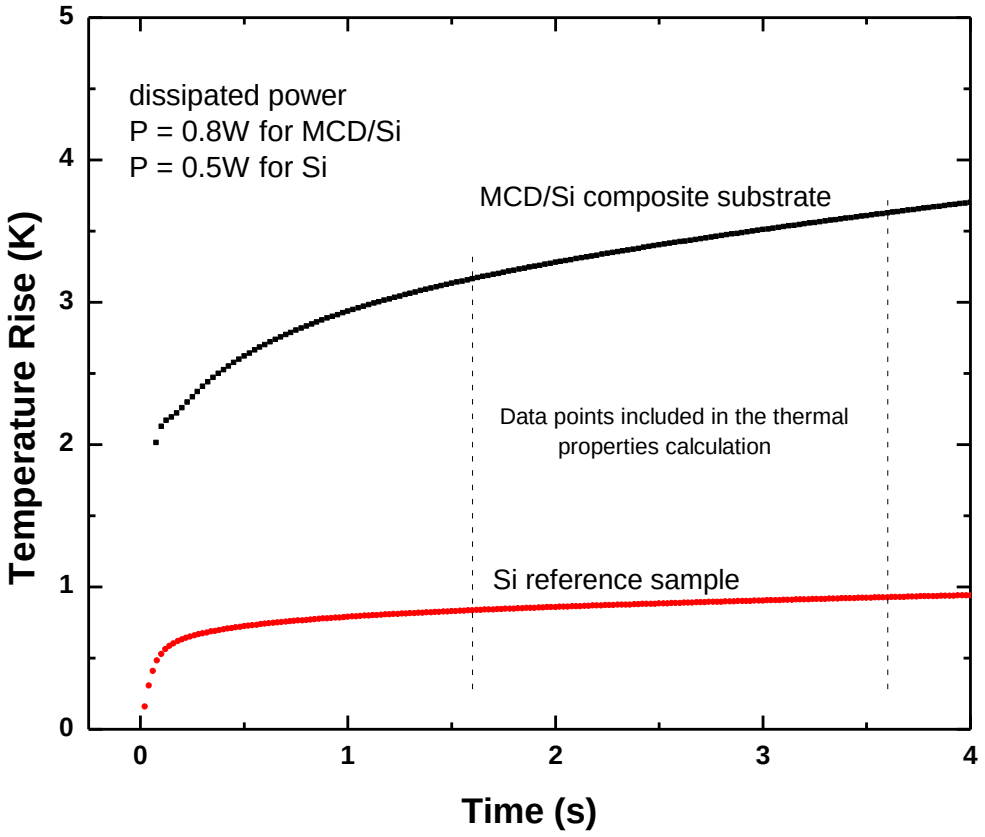


Figure 4.6: Transient temperature rise for the MCD/Si composite substrate and reference Si sample measured by the TPS technique. Reprinted with permission from V. Goyal, S. Subrina, D. Nika, and A.A. Balandin, "Reduced Thermal Resistance of the Silicon - Synthetic Diamond Composite Substrates at Elevated Temperatures," *Appl. Phys. Lett.*, vol. 97, 031904, 2010 © 2010 American Institute of Physics.

Figure 4.8 shows the measured effective thermal conductivity, K_{eff} as a function of temperature, T for reference (bulk) Si wafer, two MCD/Si and two UNCD/Si composite wafers, using the "hot disk" technique. Suggested reference K-T values for Si from

literature (red circles) have been added to the plot [29] affirming credibility of the apparatus and attesting to the accuracy of our measurements.

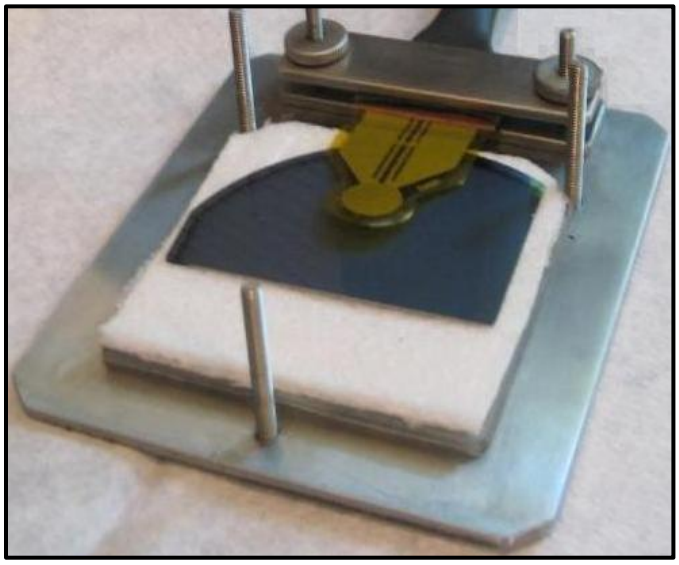


Figure 4.7: Schematic of sample-sensor arrangement in TPS technique. Nano-Device Laboratory, UCR.

The systematic error was found to be +/- 3% and is shown by error bars. The Si wafer's *K* scales as ~1/*T*, which is expected for semiconductor crystals near RT. The $K_{eff}(T)$ dependence for MCD/Si (UNCD/Si) is distinctively different. The thermal conductivity of the composite Si-Di substrates actually grows with temperature from RT to ~100-200^{o}C, depending on the grain size and thickness of the diamond layer. The unexpected observation is that the crossover point, where K_{eff} of the composite substrates

becomes larger than that of conventional Si wafers, is reached at rather low $T \approx 75\text{-}150^{o}C$. The examined MCD/Si substrates start to outperform Si wafers sooner than UNCD/Si substrates. The crossover point shifts to lower *T* with increasing thickness of MCD layer. This is an important observation, which means that the composite Si/Di wafers can be less thermally resistive at the operating temperature of the state-of-the-art electronic chips and high-power devices. The operation temperature of Si electronic chips is near or even higher than this temperature and is anticipated to increase further with chip density. The cross-over for ~1 μm MCD – Si wafers occur at $T \sim 100^{o}C$. The lower thermal conductivity of ~1 μm MCD as compared to 7 μm MCD corresponds to the grain size effect on thermal conductivity, as the grains get larger the thermal conductivity increases until the grain sizes are larger than ~20 μm [30].

As shown in Figure 4.8, two UNCD/Si wafers with nearly same grain sizes but different film thickness: 1μm and 2μm have different thermal conductivity and hence they cross over even farther at $T \sim 130\ ^{o}C$ and $\sim 150\ ^{0}C$ respectively. This suggests that the thermal conductivity of diamond-Si composite wafers decrease with increase in thickness of the diamond film. It is appropriate to mention that the thermal conductivity of a composite material is a combination of the thermal conductivities of the constituents. The obtained results are very important from practical point of view and the parameters like diamond film thickness, grain size, etc. can be tuned (optimized) according to the application.

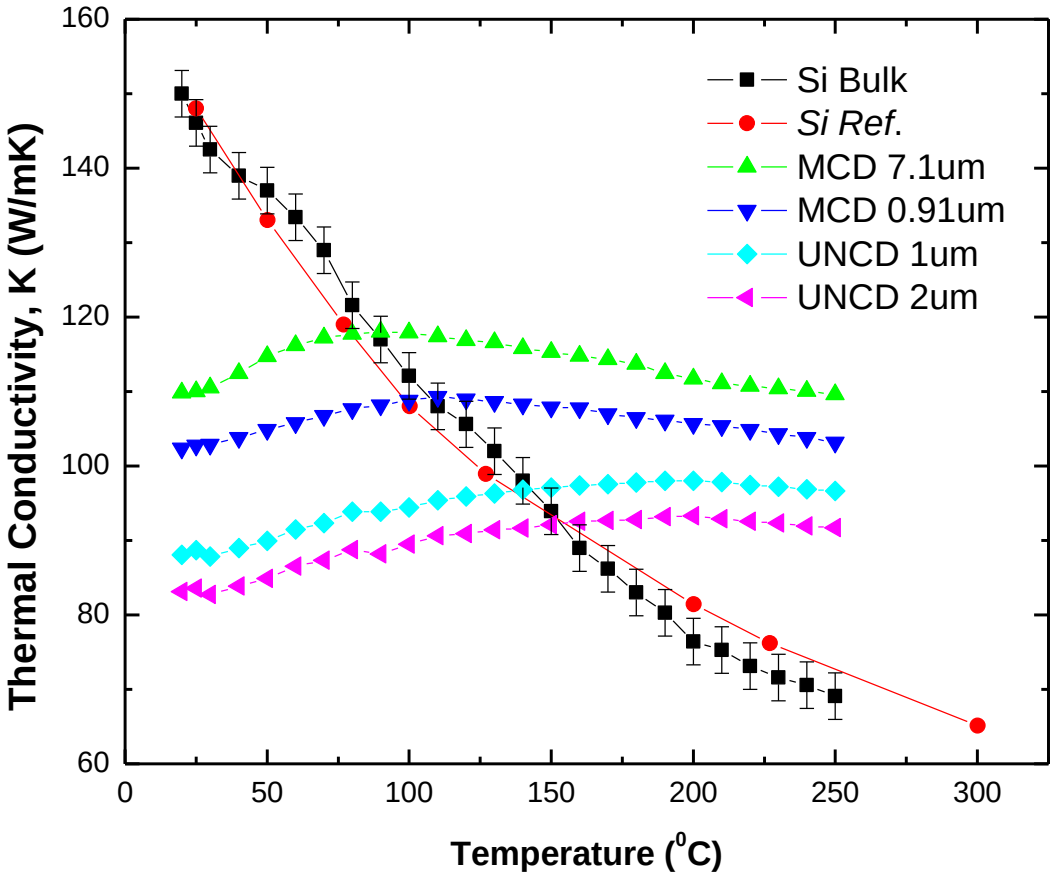


Figure 4.8: Measured effective thermal conductivity of UNCD/Si, MCD/Si and reference Si substrates as a function of temperature. Reprinted with permission from V. Goyal, S. Subrina, D. Nika, and A.A. Balandin, "Reduced Thermal Resistance of the Silicon - Synthetic Diamond Composite Substrates at Elevated Temperatures," *Appl. Phys. Lett.* vol. 97, 031904, 2010. © 2010 American Institute of Physics.

4.4 Temperature Dependence of Thermal Conductivity of Si/Di and Bulk Si

The physics behind the lower thermal resistivity of Si/Di wafers at elevated temperatures is related to differences in *K(T)* dependence of crystalline Si and UNCD or MCD. In bulk crystals thermal conductivity is limited by the crystal anharmonicity via the phonon Umklapp scattering, which results in 1/*T* scaling. The *1/T* decrease is characteristic for low-defect bulk crystals at high temperatures. In polycrystalline materials *K* increases with *T* or depends only weakly on *T*. The changed *T* dependence can be explained by various theoretical models, e.g. using a conventional Callaway-Klemens approach, where scattering on grains is the dominant phonon relaxation mechanism [31-32], or the phonon-hopping model [33], which predicts higher rates of the phonon grain-to-grain transmissions with increasing *T*. For a large variety of polycrystalline CVD films with great difference in quality, a general relationship $K \sim 1/T^x$ above room temperature has been established [16] with the exponent *x* ranging from $0.17 < x < 1.02$. The smaller *x* values correspond to more defective films. The phonon scattering from the grain boundaries plays an important role at low *T* [34-36].

The effective thermal conductivity of MCD/Si shows a flattened peak at *T*~100 ^{0}C, and rolls off slower than 1/*T*. The $K_{eff}(T)$ dependence for UNCD/Si samples is different from that in bulk crystals and MCD. It does not have a clear maximum and monotonically increase with *T* till it saturates around *T*~200 ^{0}C. The monotonic *K* increase with temperature is similar to that in the disordered materials. The cross-over temperature is higher for UNCD/Si samples owing to lower thermal conductivity of

UNCD because of its smaller grain sizes. The sp^2 content present at the grain boundaries in UNCD films also strongly affects its thermal conduction.

4.5 Thermal Boundary Resistance (TBR) at UNCD/Si and MCD/Si Interfaces

The correlation of the material parameters with the thermal properties is important for development of the chip design with improved thermal management and carrier mobility. The thermal boundary resistance at the interface between silicon and polycrystalline diamond is one of such parameters. We measured the thermal conductivity and thermal boundary resistance (TBR) at the interface between UNCD and silicon. In order to find TBR at the interface between diamond and Si one can measure the thermal conductivity of two Si - diamond heterostructures with different thickness and solve a system of equations

$$\frac{H_{Si+dn}}{K_{Si+dn}} = \frac{H_{Si}}{K_{Si}} + \frac{H_{dn}}{K_d} + R_{Bd}, \qquad [4.2]$$

where H_{Si+dn} is the thickness of the Si - diamond wafer, for the two samples with n = 1, 2, respectively. H_{Si} is the thickness of the Si layer in either of the wafers, H_{dn} is the thickness of the diamond layer in the two wafer respectively. K_{Si+dn} is the effective thermal conductivity of the Si/Di wafer for the two samples with n = 1, 2 respectively, K_{Si} is the thermal conductivity of Si, K_d is the thermal conductivity of diamond, and R_{Bd} is the TBR (see Figure 4.9). Since the total thickness of each wafer was

significantly larger than the thickness of the diamond films, we assumed that $H_{Si+dn} = H_{Si}$. Two UNCD wafers with different diamond-layer thickness: 1.17+/-0.03 µm and 1.77+/-0.06 µm. Both wafers had the same diameter of 100 mm. The overall thickness of each wafer was measured to be 530+/-3 µm.

Figure 4.10 shows the calculated TBR at the interface between diamond and silicon using the effective thermal conductivity values of Si/Di and Si as measured using the TPS technique. The TBR value is (8.9+/-2.2) x 10^{-7} m^2K/W at T = 20 ^{0}C and it decreases with increasing temperature. At T = 80 ^{0}C TBR is equal to (1.5+/-1.7) x 10^{-7} m^2K/W. Characteristic uncertainty in the measurement is indicated by the error bars.

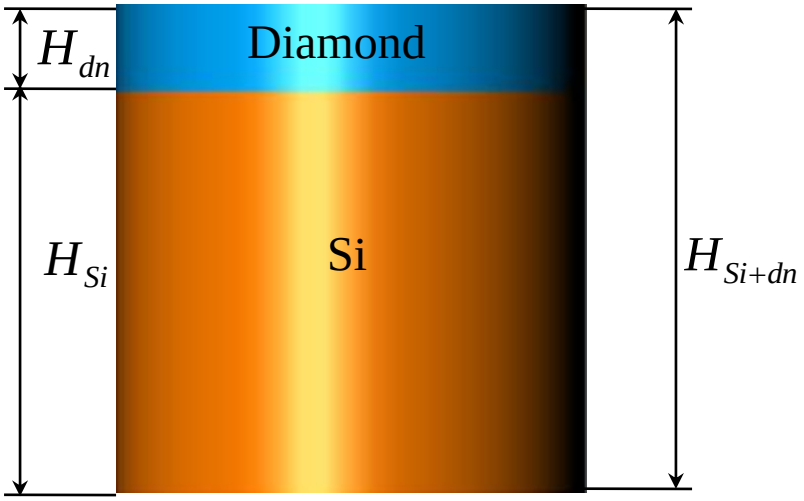


Figure 4.9: Schematic of Si - diamond wafers used for measurements of the thermal boundary resistance. Reprinted with permission from V. Goyal, D. Kotchetkov, S. Subrina, M. Rahman, and A.A. Balandin, "Thermal Conduction through Synthetic Diamond-Silicon Heterostructures," Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm), 2010 12th IEEE Intersociety Conference © 2010 IEEE.

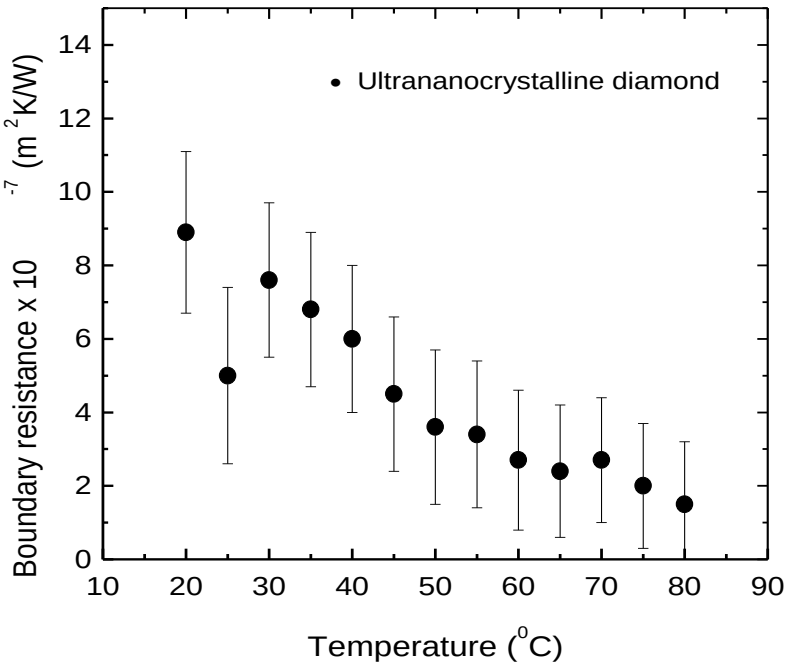


Figure 4.10: Thermal boundary resistance between UNCD/Si interfaces. Reprinted with permission from V. Goyal, D. Kotchetkov, S. Subrina, M. Rahman, and A.A. Balandin, "Thermal Conduction through Synthetic Diamond-Silicon Heterostructures," Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm), 2010 12th IEEE Intersociety Conference © 2010 IEEE.

A rather large uncertainty in the extracted TBR values is related to the non-uniformity and uncertainties in the thickness of the synthetic diamond layer as well as standard (systematic) error associated with the hot-disk measurement procedure [37].

To understand the effect of the interface imperfections on the measured TBR values we calculated TBR using the two most common approaches: the acoustic mismatch model (AMM) and the diffusive mismatch model (DMM) [38]. The acoustic mismatch model assumes no scattering of phonons at the interface between two solids

and the diffusive mismatch model assumes that all the phonons diffusely scatter at the interface. For both the models the thermal boundary resistance between Si and UNCD can be calculated using expression

$$R_{Bd} = \left\{ \frac{1}{2} \sum_j c_{1,j} \Gamma_{1,j} \int_0^{\omega_1^{Debye}} \hbar\omega \frac{dN_{1,j}(\omega,T)}{dT} d\omega \right\}^{-1} \quad [4.3]$$

where ω is the phonon's frequency, c is the speed of sound in the material, $\hbar$ is the reduced Planck constant, T is the temperature, Γ is the transmission coefficient, dN is the phonon density of states, and ω^{Debye} is the Debye frequency. The index i refers to Si; the index j refers to the phonon mode (transverse or longitudinal). The phonon density of states is expressed by

$$N_{1,j}(\omega,T) = \frac{\omega^2}{2\pi^2 c_{1,j}^3 \left[\exp\left(\frac{\hbar\omega}{k_B T} \right) - 1 \right]} \quad [4.4]$$

where k_B is Boltzman constant, and the transmission coefficient can be written as

$$\Gamma_{1,j} = \int_0^{\frac{\pi}{2}} \alpha_{1\to 2}(\theta, j) \cos\theta \sin\theta d\theta, \quad [4.5]$$

where α is the transmission probability, and the index 2 refers to UNCD. The Debye frequency is given by

$$\omega^{Debye} = \frac{k_B \theta^{Debye}}{\hbar} \quad [4.6]$$

where θ^{Debye} is the Debye temperature. This parameter equals 645 K for Si [6], which corresponds to the value 8.44 x 10^{13} Hz for the Debye frequency.

To simplify computations, one can assign the Debye frequency to be infinite, then the equation [4.2] transforms to

$$R_{Bd} = \left\{ \frac{\pi^2}{15} \frac{k_B^4}{\hbar^3} \sum_j c_{1,j}^{-2} \Gamma_{1,j} \right\}^{-1} \times T^{-3} \qquad [4.7]$$

The difference between the acoustic mismatch model and the diffusive mismatch model is in definition of the transmission probability $\alpha_{1\to 2}$. In the acoustic mismatch model it is given by

$$\alpha_{1\to 2} = \frac{4 Z_1 Z_2}{\left(Z_1 + Z_2\right)^2} \qquad [4.8]$$

where $Z=\rho c$ is the acoustic impedance of the material equal to the product of the mass density ρ and the speed of sound c. In the diffusive mismatch model the transmission probability does not depend on the impedance and is given by

$$\alpha_{1\to 2} = \frac{c_2^{-2}}{c_1^{-2}} \qquad [4.9]$$

To calculate the theoretical values of TBR we used the following parameters: 2.33 g/cm^3 and 3.47 g/cm^3 for the mass densities of Si [6] and UNCD [39], respectively, and 12.30 x 10^5 cm/s, 5.33 x 10^5 cm/s, and 8.97 x 10^5 cm/s for the sound velocities of UNCD

[39], the transverse speed of sound in Si [6], and the longitudinal speed of sound in Si [6], respectively.

Figure 4.11 shows a comparison between the measured values of TBR and the values computed according to both models. The theoretical values are substantially lower than the experimental ones. Since both models assume either perfectly specular or perfectly diffuse phonon scattering they do not account for the interface imperfections and deviations from the model assumptions. Our modeling and experimental data suggest that the interface quality in UNCD/Si structures, in terms of heat transport, is still far from being perfect and suitable for many envisioned applications. Such large discrepancies between the theoretically predicted TBR for the ideal-interface phonon scattering (either perfectly specular or perfectly diffuse) and experimental results for systems with far-from-perfect interfaces are rather typical [40] which has been shown in the Figure 4.11.

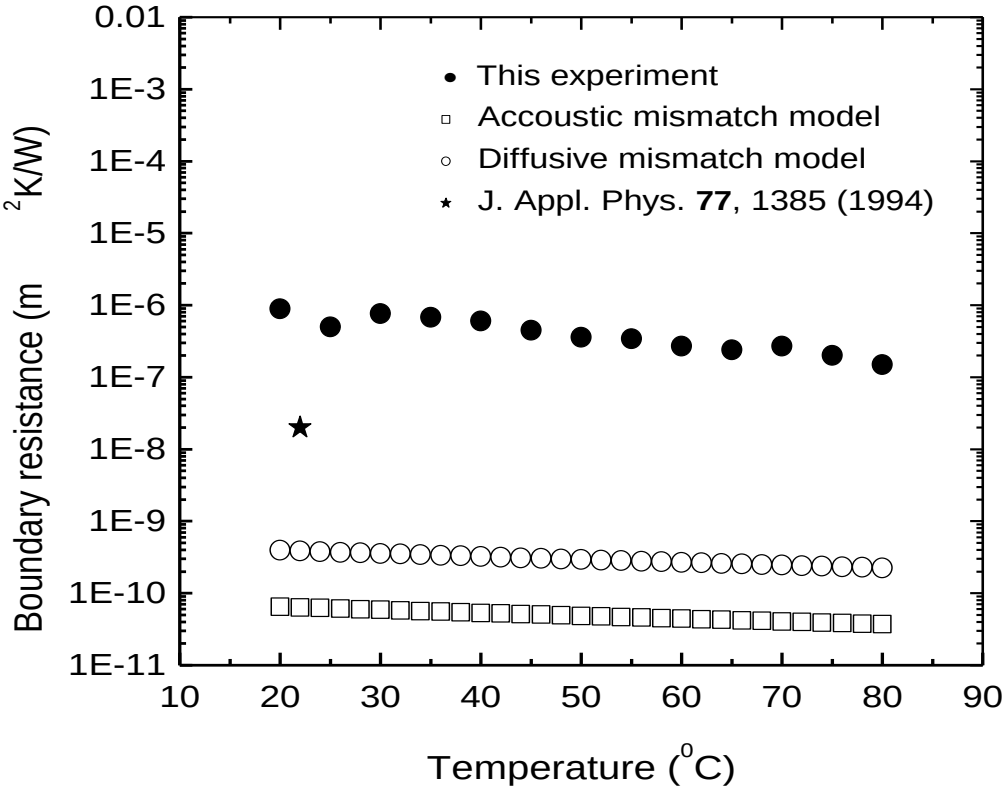


Figure 4.11: Comparison of the data for the thermal boundary resistance measured in the current experiment with previously reported data and theoretical predictions. Reprinted with permission from V. Goyal, D. Kotchetkov, S. Subrina, M. Rahman, and A.A. Balandin, "Thermal Conduction through Synthetic Diamond-Silicon Heterostructures," Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm), 2010 12th IEEE Intersociety Conference © 2010 IEEE.

To analyze our results we determined the thermal conductivity, K_{Di}, of the synthetic diamond layers themselves from the equation $L/K_{eff}=L_{Si}/K_{Si}+L_{Di}/K_{Di}$, where $L=L_{Si}+L_{Di}$ is the total thickness of the composite substrate, K_{Si} is the thermal conductivity of the Si wafer, and L_{Si} (L_{Di}) is the thickness of the Si wafer (diamond layer). Here we

neglected TBR at the Si/Di interface. It is at least an order of magnitude smaller than L_{Si}/K_{Si} or L_{Di}/K_{Di} as estimated by applying the above equation to two samples with the same type of diamond layer but different thickness L_{Di}. We then calculated the interfacial grain-to-grain thermal conductance $G=(K_D/d)[1/(K_D/K_{Di}-1)]$, where K_D is the thermal conductivity inside the grain, which is assumed to be equal to the crystalline diamond's bulk value [41]. For our UNCD layers we found G~50-100 MW/m^{2}K for the average grain diameters d~5-10 nm at RT. For UNCD, G grows with T and can be approximated as $G(T)$[MW/m^{2}K]≈81.2+1.65×10$^{-4}T^3$ [^{o}C] for grain size d~5nm and for our MCD layers $G(T)$[MW/m^{2}K]≈0.029+1.05×10$^{-4}T^3$ [^{o}C] for grain size d~1μm. The $G(T)$~T^3 dependence is consistent with the Kapitza thermal resistance behavior [38] for both UNCD and MCD as shown in Figure 4.12 (a) and (b) [47]. The obtained values fall within the conventionally accepted range G~20-200 MW/m^{2}K for the interface conductance between dissimilar materials near RT [5]. Our analysis suggests that Si-Di composite substrates even with non-perfect grain interfaces perform better for heat removal at elevated temperature than Si.

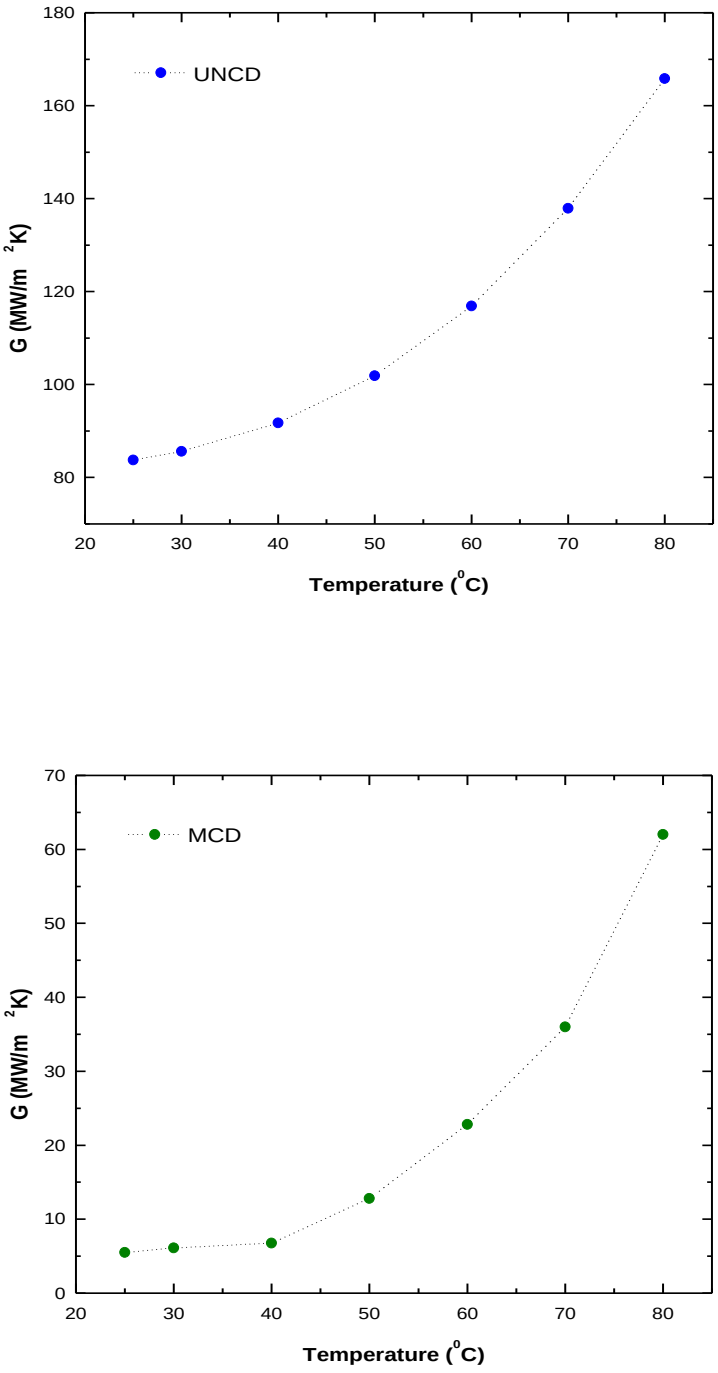


Figure 4.12: Thermal Conductance for (a) UNCD/Si and (b) MCD/Si interfaces. Filled circles represent the calculated values. Connecting line is to guide the eyes.

4.6 Mobility Enhancement in Si/Di Substrates

To obtain estimates for the electron mobility enhancement as a result of higher K_{eff} of Si-Di substrates we simulated *T* profiles in the examined wafers. The heat diffusion equation for given structures was solved numerically by the finite-element method using COMSOL software. The devices were modeled as heat sources with the power density and geometry chosen in such a way so that the resulting temperature rise is close to the typical values in state-of-the-art chips. In our model we approximate several active devices as rectangular heat generating elements on Si as well as on diamond/Si composite substrates. Each source has the width and thickness of 50 nm and 25 nm, respectively; and is separated from each other by 10 μm. The linear power density of each active channel was set to 0.3 W/mm. The thickness of Si and MCD/Si substrates is 500 μm. A conventional heat sink is attached to the device structure at the bottom to maintain constant temperature at 300K. Figure 4.13 shows the schematic of a circuit on Si substrate. The external surfaces were modeled as insulated from the environment. The heat conduction was modeled by solving numerically Fourier's law

$$-\nabla \cdot (k\nabla T) = Q \qquad [4.10]$$

where *Q* is the heat source, which is defined as the heat energy generated within a unit volume per unit time, *T* is the absolute temperature and *k* is the thermal conductivity.

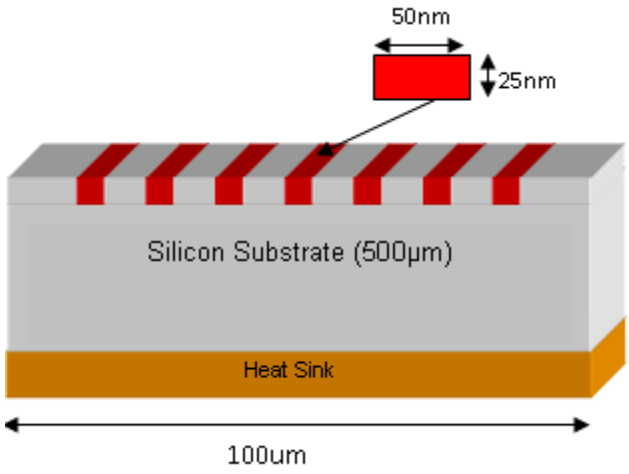
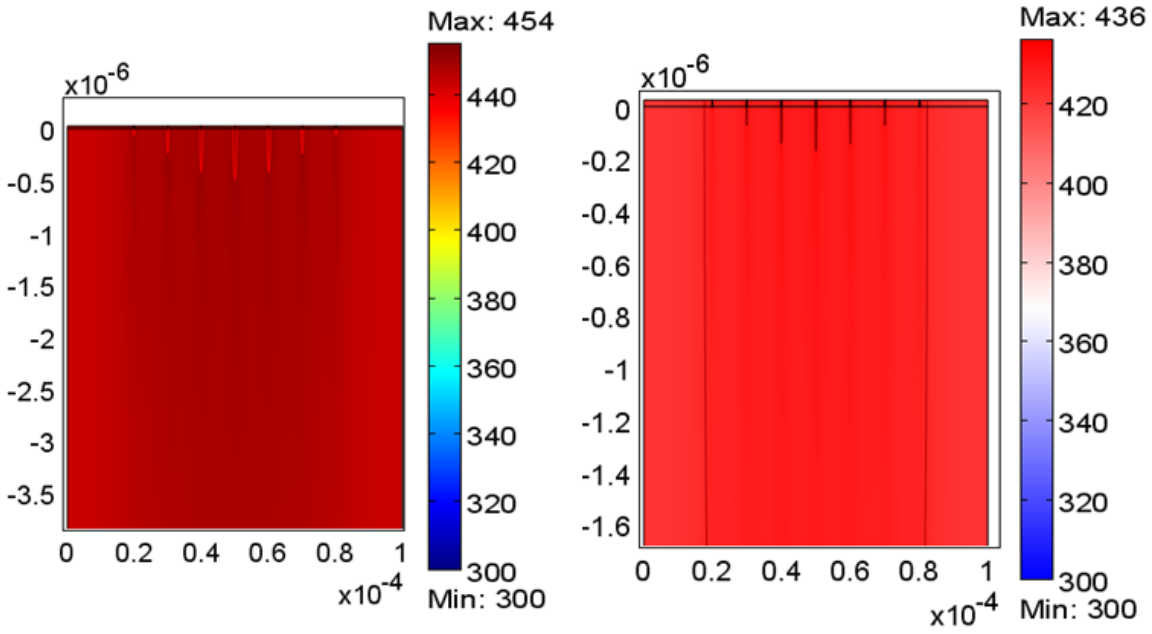


Figure 4.13: Schematic of simulation structure with seven active devices on Si wafer.

The conventional Si wafers were then replaced with the Si-Di substrates and modeled with the experimentally determined K_{eff}. The actual $K_{eff}(T)$ dependence was taken into account. The difference in the device-channel temperature rise, ΔT_m, between Si wafers and Si-Di substrates (see Figure 4.14 (a) and (b)) was translated into the carrier mobility values using the expression

$$\mu(T) \sim T^{n} \qquad [4.10]$$

where n~2.42 for Si [42-43]. We found that for realistic chip parameters one can obtain a reduction ΔT_m~20-40^{o}C, which can result in up to ~20% mobility increase. The μ increase can be made larger via improvement of Si-Di substrates quality, increase in L_{Di} for MCD and increase in G for UNCD and MCD.



(a) (b)

Figure 4.14: Temperature distribution across the given circuit with seven active devices on (a) Si substrate and (b) Si/Di substrates. Temperature is indicated in Kelvin. Simulation results are courtesy of Dr. Samia Subrina, Nano-Device Laboratory, UCR.

The expected increase in the chips' operation temperature will also result in greater improvement because the difference K_{eff} of Si-Di and Si becomes larger. The currently used methods for the mobility improvement in Si CMOS use SiGe alloys to strain the device channels [44]. The alloys are characterized by very low K [45]. The mobility, which can be achieved in chips implemented on Si-Di substrates, will not be prone to degradation due to higher thermal resistance.

4.7 Summary

In conclusion, we experimentally investigated the effective thermal conductivity of UNCD films and MCD films deposited on Si wafers using the TPS method. The temperature dependence of the thermal conductivity of the UNCD and MCD films was compared with that of Si. It was shown that the temperature dependence of the thermal conductivity of UNCD/Si and MCD/Si are noticeably different from that for Si, and can be adequately described by the phonon-hopping model. We demonstrated that composite Si-diamond substrates, which are more thermally resistive than Si at RT, *outperform* Si at elevated temperatures characteristic for operation of the state-of-the-art electronics. The benefits of the composite substrates increase with the chips' growing power density and operation temperatures. We elucidated physical processes leading to the improved thermal properties of the composite substrates, and outlined the strategy for achieving mobility enhancement via thermal, i.e. phonon flux, engineering.

Our simulation results show that the incorporation of MCD/Si composite wafers not only leads to substantial reduction in temperature of the hot spots but also corresponds to increase in the carrier mobility by ~ 20% for a given structure. The obtained results shed light on the dependence of thermal conductivity of synthetic diamond/Si composites on the grain size, the thickness of diamond layer and the TBR at the interfaces. In principle, as the technology develops, one can optimize the diamond layer thickness, grain size, and interfacial grain-to-grain thermal conductance and interface TBR to tune the thermal conductivity and interface smoothness to suit the requirement. Another benefit of using diamond with Si is a continuing drive for carbon

electronics, which includes carbon nanotubes, graphene and diamond-like carbon. Carbon materials are characterized by a very wide range of *K*, from the highest in graphene to the lowest in disordered carbons [46], and can provide both thermally conductive and insulating interfaces.

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Chapter 5

Thermal Conductivity of Directly Integrated Nanocrystalline Diamond Films with GaN

5.1 Introduction

GaN have attracted major attention owing to its wide range of potential applications. GaN, with a large band gap of 3.4eV, possesses a very high breakdown voltage of 3×10^6 Vcm^{-1} and an extremely high peak and saturation velocity of 3×10^7 cm s^{-1} and 1.5×10^7 cm s^{-1}, respectively [1]. These unique properties along with the high electron mobility of 2019 cm^2 V^{-1} s^{-1} observed in AlGaN/GaN heterostructures [2] make GaN as a superior material to Si, Ge and GaAs for high-temperature/high-power electronic devices, ultrahigh power switches, and microwave-power sources [3]. However, self-heating limits the continuing development of GaN-based technology [4, 5]. It has been illustrated that the significant temperature rise in high-power AlGaN/GaN HFETs is on order of ~180 ^{0}C [6] which is assumed to increase further with increased current densities and shrinking device geometries. For this reason, reliable performance of such devices depends on the heat dissipation in the device active regions, which, in turn, depends on the thermal conductivity of GaN and the common substrates used for its growth (e.g. silicon, sapphire, SiC). Most recently, GaN-on-diamond wafers have been proposed as alternatives to conventional SiC-GaN offering improved thermal management [7].

Numerous approaches have been explored to integrate diamond with GaN including wafer-bonding, which involves either physically bonding GaN substrate with diamond wafers through some interlayer [8] or by directly depositing diamond films on GaN [9]. In the first case, the bonding process is critical, costly and involves an additional dielectric adhesive layer of ~50 nm. This interlayer of dissimilar material presents a thermal barrier making it less efficient in the heat transfer. In the second case, due to the high substrate temperature requirement of diamond deposition process (~800 ^{o}C), it has been found that GaN starts to degrade either due to diffusion of carbon in to the GaN lattice or loss of N from the GaN lattice leading to degradation of performance of overall semiconductor layers deposited on GaN. Moreover, it has been shown that lowering the temperature below 600 ^{0}C using conventional H_2/CH_4 based growth chemistry results in growth of poor quality diamond. It is therefore very important to achieve good quality diamond film on GaN substrate at low substrate temperatures (400-500 ^{o}C).

In this work, in collaboration with Argonne National Lab (ANL), we present a novel approach based on nanocrystalline diamond (NCD) films growth using $Ar/CH_4/H_2$ gas chemistry to deposit good quality NCD film directly on the GaN substrate at low substrate temperatures (450-500 ^{0}C), with thermal conductivity better than that of GaN at elevated temperatures. The crossover point, when the effective thermal conductivity of NCD/GaN composite substrates outperforms that of GaN, is reached in the range T~95-125 ^{0}C depending on the thickness of the NCD films deposited. The temperature when the NCD/GaN substrates become high thermally conductive is relatively lower than the operating temperature (T~180 ^{0}C) of GaN based HFETs which clearly states the specific

advantage offered by thin NCD films for efficient thermal management of GaN based high power/high temperature devices.

5.2 Sample Preparation and Characterization

Different thickness of NCD films were grown on free standing, single crystal GaN substrates (480 micron thick) to study the effect of the NCD film thickness on the thermal conductivity. Growth of NCD films were performed in 915 MHz large-area microwave plasma chemical vapor deposition (MPCVD) system (DiamoTek 1800 series 915 MHz, 10 KW from Lambda Technologies Inc.) at the Center for Nanoscale Materials at Argonne National Lab (ANL). Prior to growth, GaN substrates were deposited with 10 nm tungsten layer using sputtering followed by seeding treatment using commercially available nanodiamond containing solution (source ITC, Raleigh, NC). This is a part of standard process that has been developed at ANL for the growth of low temperature nanocrystalline diamond film on a given substrate [10]. Argon rich environment consisting of $Ar/CH_4/H_2$ chemistry was used to grow NCD films unlike the conventional hydrogen rich environment using H_2/CH_4 gas chemistry which is used for growth of NCD films. It has been observed that MPCVD process results in the systematic increase in grain size of ultrananocrystalline diamond (UNCD) with increase in hydrogen concentration due to the suppression of renucleation rate leading to transition of UNCD in to nanocrystalline and eventually in the microcrystalline diamond phase [11]. In the present case, we have observed a similar trend in grain size even at low (450^oC) substrate

temperature. More importantly, we were able to tune diamond grain size to ~200 nm using 4.5% hydrogen in to the Ar/CH_4 gas mixture without coarsening effect. This allowed us to deposit NCD films by varying NCD film thickness without any measurable change in the average grain size. Figure 5.1 show the high-resolution field-emission scanning electron microscope (XL-30 FEG) scans of two different thickness NCD films (a) 150 nm and (b) 300 nm, on GaN, respectively. The images reveal that the grain sizes for both the NCD films (with different thicknesses) are on the order of ~200 nm which signifies no grain size change with change in thickness, which is not the case for microcrystalline diamond (MCD). The thickness of the NCD films was verified using cross-sectional FIB slicing and SEM imaging as shown in Figure 5.2. A thin a layer of Pt was deposited locally on the NCD using FIB to get much better edge resolution by avoiding redeposition during FIB cut.

It is believed that Ar rich gas chemistry of growing NCD at low temperature is more favorable for achieving NCD growth on GaN as opposed to H_2 rich method since that way we have not only reduced the total concentration of reactive atomic hydrogen in the growth chamber but also slowed down the reaction kinetics due to the retarded surface diffusion process at low temperatures, both of these facts are important in achieving good quality NCD growth on GaN without any adverse affect and keeping the GaN structure unaffected.

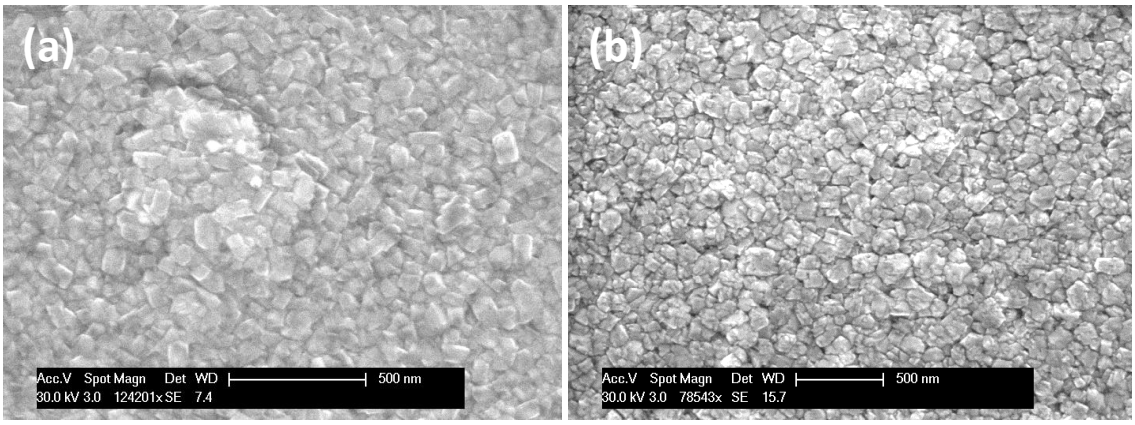

Figure 5.1: Top-view SEM images of two NCD films with different thicknesses (a) 150 nm and (b) 300 nm with similar grain size of ~150nm

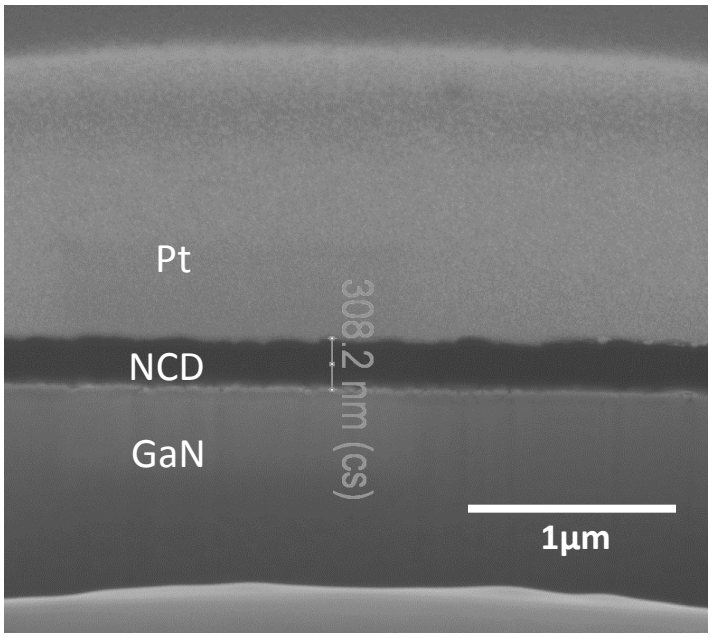

Figure 5.2: Focused ion beam (FIB) cross-section SEM image of NCD/GaN substrate confirming the thickness of NCD film. Image is courtesy of Dr. Anirudh V. Sumant, Argonne National Laboratory.

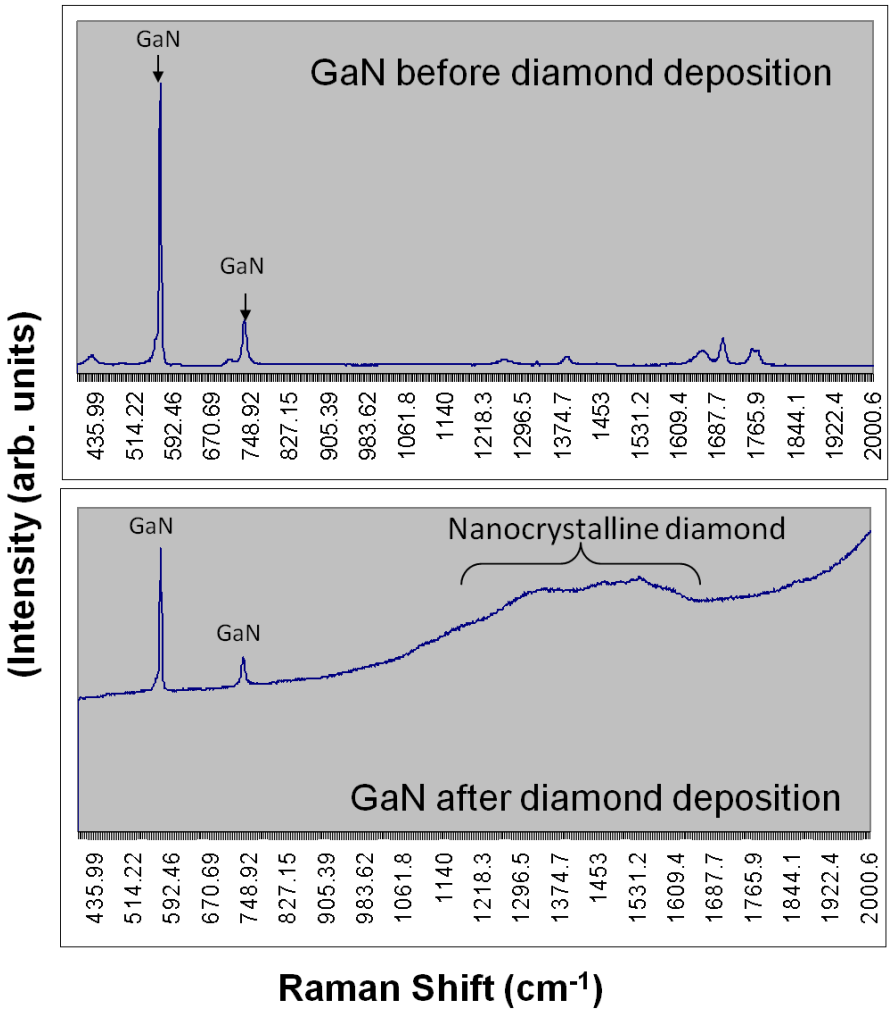

Figure 5.3: Visible Raman (λ: 632.8 nm) spectra of GaN substrate before and after NCD deposition demonstrating no loss of GaN structure after diamond deposition. Image is courtesy of Dr. Anirudh V. Sumant, Argonne National Laboratory.

Raman spectroscopy was performed to assay annealing induced damage that may have occurred in GaN during diamond deposition. Raman spectroscopy of GaN substrates before and after the growth of NCD film confirmed that the intrinsic structure of GaN was indeed well preserved and does not change during the diamond growth process (see Figure 5.3).

Raman spectroscopy has also been used extensively for the characterization of diamond films to better understand the sp^3/sp^2 ratio. However, in case of nanocrystalline diamond, it is well-known that due to smaller grain size, and increased grain boundary volume, the visible Raman spectra is mostly dominated by sp^2 bonded carbon due to uneven Raman scattering cross-section for sp^2 and sp^3 bonded carbon. Therefore it is difficult to interpret real sp^3/sp^2 ratio in nanocrystalline diamond quantitatively just based on Raman data. In such cases electronic methods rather than optical method is more sensitive such as near edge x-ray absorption spectroscopy (NEXAFS) based on synchrotron x-rays. Unlike Raman spectroscopy, it is equally sensitive to sp^3- and sp^2-bonded carbon as well as other bonding forms. Since NEXAFS probes the core-hole perturbed local density of unoccupied states, the spectra obtained from diamond and graphite are very different due to the distinct structures of their unoccupied electronic states. NEXAFS spectra were taken at Brookheaven National Laboratory in total electron yield mode. Figure 5.4 shows the C 1s NEXAFS spectra taken on NCD film deposited on GaN confirming its good quality.

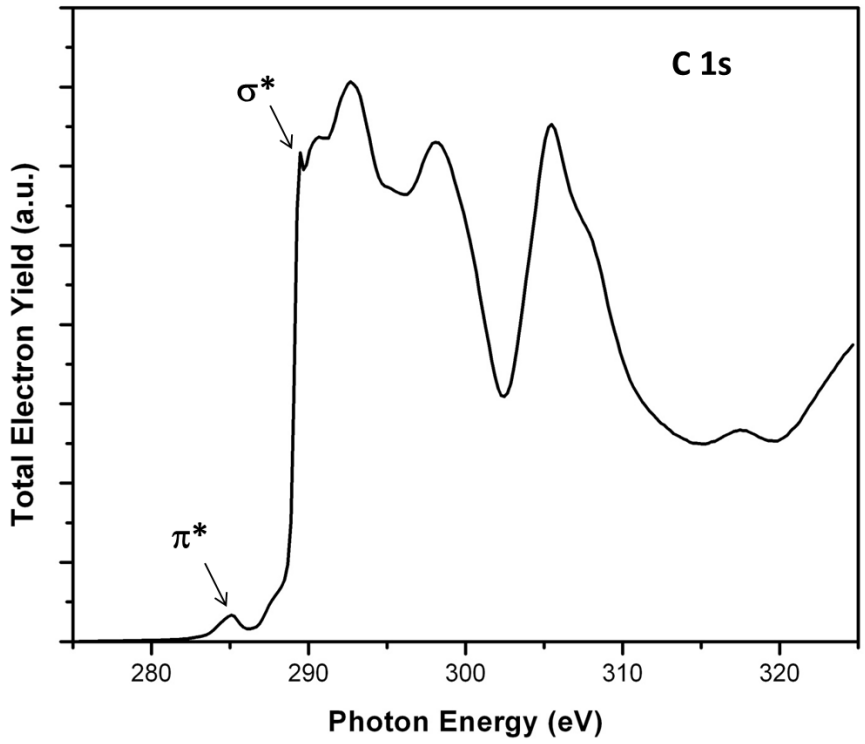

Figure 5.4: C 1s NEXAFS spectra taken on NCD film deposited on GaN. Image is courtesy of Dr. Anirudh V. Sumant, Argonne National Laboratory.

5.3 Thermal Conductivity Measurements on NCD/GaN Wafers

The thermal conductivity measurements on NDC/GaN and reference substrates were carried out using the transient plane source (TPS) hot disk technique [12]. Laser-flash (Netszch LFA) technique was also used to measure thermal conductivity of reference GaN substrates. Both techniques have been previously "calibrated" with the 3-ω method,

[13-14] which is considered to be a standard technique for measurement of thermal conductivity of thin films. We have previously successfully used the TPS measurements for UNCD and micro crystalline (MCD) diamond films on Si [15]. The electrical TPS technique can measure the average in-plane thermal conductivity whereas the optical laser-flash technique set-up allows to measure the average cross-plane K of the sample under investigation.

Figure 5.5 presents the effective thermal conductivity as a function of temperature $K_{eff}(T)$ for the two NCD/GaN samples with different thickness NCD films measured using TPS technique, and for the reference GaN substrate measured by TPS technique as well as laser-flash technique [16]. A comparison with K values for GaN from two different techniques indicates an excellent agreement and attests to the accuracy of our measurements. RT thermal conductivity of reference GaN was found to be $K \sim 136$ (+/- 1.8) W/mK. This K value is highly dependent on the quality (defects, dislocations, impurities/doping concentration, etc.) of GaN [17].

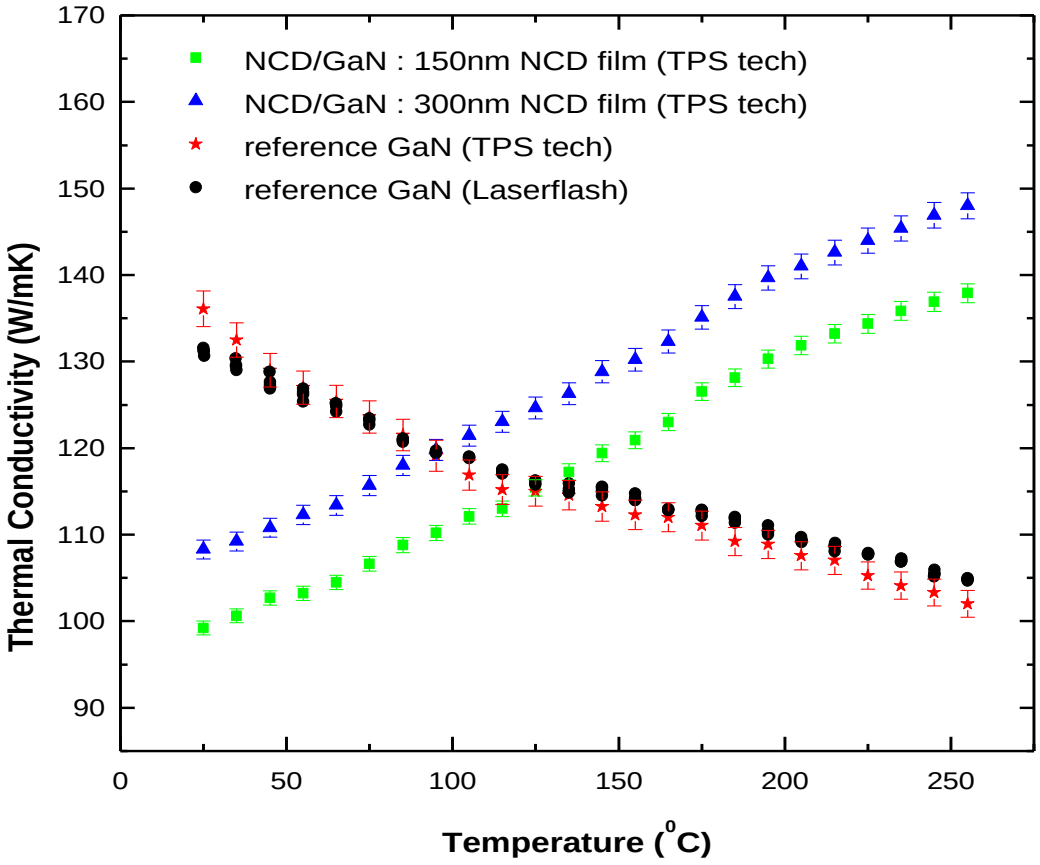

Figure 5.5: Thermal conductivity as a function of temperature for two NCD/GaN composite substrates, as well as for the reference GaN wafer measured by TPS and laser-flash technique. The error bars represent the data scattering based on "10" measurements taken at each temperature.

5.4 Results and Discussion

As shown in Figure 5.4 the thermal conductivity of the NCD/GaN substrates is lower than that of GaN at RT, but it outperforms at elevated temperatures. The monotonic

decrease in GaN substrate's K with T is characteristic for semiconductor materials where thermal transport is limited by the crystal inharmonicity via the phonon Umklapp scattering, which results in $1/T$ dependence. On the other hand, the $K_{eff}(T)$ dependence for NCD/GaN is distinctively different. The effective thermal conductivity of the NCD/GaN composite substrates increases with temperature from RT to the measurement temperature range. This changed T dependence in polycrystalline materials such as NCD can be explained either by the conventional Callaway–Klemens approach, where the dominant mechanism restricting the thermal transport is the phonon scattering at the grains boundaries [18, 19] or by the phonon-hopping model proposed by Braginsky *et al* [20] which assumes that the phonon transport inside the grain follows the "*bulk rules*" while at the grain boundaries the phonon transition rate from one grain to another through the inter-grain boundary increases with increasing T. This difference in $K(T)$ dependence of crystalline GaN and polycrystalline NCD results in a crossover point where the effective thermal conductivity of NCD/GaN substrates out passes that of reference GaN substrate. The crossover point is reached at rather low T~124 ^{0}C and further shifts to a lower T~95 ^{0}C as the NCD thickness increases from 150 nm to 300 nm. This is an important observation, demonstrating that although composite NCD/GaN substrates are less thermally conductive than GaN at RT, they can be more thermally efficient at the operating temperature of the state-of-the-art GaN based HFETs (~180 ^{0}C).

Another important observation is that the effective thermal conductivity of NCD/GaN substrates increases with increase in thickness of the NCD films, which is in contrast to what was observed for UNCD/Si substrates by Goyal *et al*. [15]. This can be

attributed to the higher *intrinsic* thermal conductivity of NCD (K~ 500-1400 W/mK) [21-22] as compared to that of GaN (K~130 W/mK) [23; *this work*] which makes the effective thermal conductivity of the composite NCD/GaN wafers to increase with increase in NCD thickness. On the other hand, UNCD have very low intrinsic thermal conductivity, K~10 W/mK [23], as compared to that of Si (K~150 W/mK) [15, 24] resulting in a decrease in the effective thermal conductivity of UNCD/Si with an increase in UNCD thickness [15].

In order to understand the physics behind the thickness dependent study, we estimated the thermal conductivity in our NCD films using lattice thermal conductivity expression [26] followed by Debye assumption,

$$K = (1/3)C_s v_g \Lambda \qquad [5.1]$$

where C_s is the specific heat capacity, v_g is the group velocity and Λ is the phonon mean free path (mfp) given by

$$\Lambda = v_g \tau \qquad [5.2]$$

where τ is the relaxation time. The electronic contribution to the thermal conductivity of NCD was neglected owing to their high electrical resistivity [22]. For estimation of specific heat capacity, density and specific heat capacity were assumed to be 3.44 g/cc [21] and 0.511 J/gK corresponding to crystalline diamond [27], which gives C_s=1.8576 J/cc-K. Group velocity or the velocity of sound in NCD can be taken from ref. 22 (*17980 m/s*), or can be estimated from equation

$$\upsilon_g = \sqrt{Y/\rho} \qquad [5.3]$$

where Y is the Young's modulus which is *~1120 GPa* for NCD [21], and ρ is the density (3.44 g/cc); which gives υ_g *~ 18000 m/s*. For NCD, the phonon mfp is limited by the grain size. For simplicity, we can approximate the phonon mfp in NCD to be equal to their grain size, *i.e.*, ~100nm. For comparison, single crystal diamond has phonon mfp *~240nm* at RT [27]. Using these values, the lattice thermal conductivity of NCD can be calculated to be *K~1110* W/mK (at RT). These theoretically estimated values of thermal conductivity of NCD, which are higher as compared to that of GaN supports our experimental observation. Moreover, the sp^2 content in our NCD films is less than that in UNCD films (as explained by the NEXAFS), which can also attribute to the superior thermal conductivity of NCD films on UNCD [16].

5.5 Summary

In conclusion, in collaboration with Argonne National Laboratory, we demonstrated a novel approach to integrate good quality nanocrystalline diamond film directly with GaN substrate at low substrate temperatures (~450 ^{o}C). Characterization of NCD/GaN composite by Raman spectroscopy revealed no observable change in the GaN structure after the diamond deposition process. We experimentally demonstrated that the thermal conductivity of NCD/GaN substrates outperform GaN (and Si) at elevated temperatures, characteristic for operation of high-power and state-of-the-art electronic devices. We elucidated the physics leading to the improved thermal properties of the composite

NCD/GaN substrates and outlined the strategy for improved thermal management of GaN electronics. The maximum achievable power density of GaN based devices can be increased further by optimizing chip-size [8] and the NCD grain size and film thickness.

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Chapter 6

Thermal Conductivity of Free Standing Polycrystalline Graphene (PCG) and Graphene Oxide (GO) Films

6.1 Introduction

Graphene, single sheet of sp^2-hybridized carbon atoms, have shown myriad of promising prospects in electronic industry since its discovery [1] owing to its extraordinary properties including superior electron mobility, thermal conductivity and mechanical strength [1-3]. At the same time, micromechanical exfoliation technique can only give minute quantities of graphene which is not feasible for mass production of graphene for practical applications. There has been a recent research interest in different methods to fabricate large area graphene including ultrahigh vacuum (UHV) chemical vapor deposition (CVD) on single crystal transition metals [4]; chemical reduction of graphene oxide [5]; ambient-pressure CVD on polycrystalline Ni films [6] and other chemical routes [7-8]. However, graphene films, or to be more precise, polycrystalline graphene films produced by these different techniques are not able to retain their excellent conductive properties. Recently, Blake *et al*. [9] suggested another approach to produce centimeter sized overlapping individual graphene and few-layer graphene flakes on top of each other deposited on glass. The ability to incorporate PCG and RGO into structures

with larger areas has recently redirected the research activities worldwide. It is crucial to have knowledge of thermal properties of polycrystalline graphene (PCG) and graphene oxide (GO) films for their possible applications in electronics, thermal management, interconnects, etc.

Interconnects is one of the most important component of semiconductor devices; most of the power on chip is consumed by interconnects. As the device size shrinks resistivity of nanometer scale metallic interconnects increases dramatically. Resistivity of the interconnect metal of choice, copper increases up to 5 times as its thickness approaches to 20 nm [10, 11]. This suggests that the thermal conductivity should also reduce by the same factor to follow Wiedemann Franz law (for metals) and should scale down to ~385/5 which is ~77 W/mK which is in line with the reported experimental data on copper thin films [12]. We have suggested that polycrystalline graphene thin films can outperform the best interconnect material, copper in terms of thermal conductivity. Only few results have been reported on thermal properties of RGO films to date [8]. In addition to above motivation, it would be very interesting for research point of view to compare thermal conductivity of PCG and RGO with that of pristine graphene and other carbon-based materials.

6.2 Sample Preparation and Characterization

For our investigation, free standing PCG films of thickness ~20 μm and free standing graphene oxide (GO) films of thickness ~1-2 μm were prepared in collaboration with Professor Geim's research group at the University of Manchester, Manchester, UK [9, 19]. The samples were prepared by direct chemical exfoliation of graphite by sonication in dimethylformamide (DMF) for ~3 hours, followed by centrifugation at 13000 rpm for 10 min to remove thick flakes. The individual graphene flakes forming the laminates had the sizes of ~100 nm while the studied films themselves had lateral dimensions on the order of few millimeters. Initial characterization of PCG and GO films was performed by scanning electron microscopy (SEM) and Raman spectroscopy. For SEM characterization, PCG and GO solutions were first deposited on SiO_2, to get better contrast.

Figure 6.1 (a) and (b) shows the film surface SEM images of PCG and GO films respectively. The SEM images reveal that the average grain size of PCG is ~100 nm x 200 nm and that RGO is ~1 μm x 1.5 μm. SEM image clearly shows the porous nature of PCG film. Measured density of the freestanding graphene paper is 0.3 g/cm^3. Therefore the layer to layer distance in spray on graphene is 7.3 (density of graphite is 2.0 to 2.2 g/cm^3) times higher than that of natural graphite (~2.2 nm). This clearly explains the higher optical transparency of thick spray on graphene films. i.e., a 20 nm real thickness corresponds to optical thickness of 9 individual graphene layers. Figure 6.2 (a) and (b) shows the optical microscopy images of PCG and GO films.

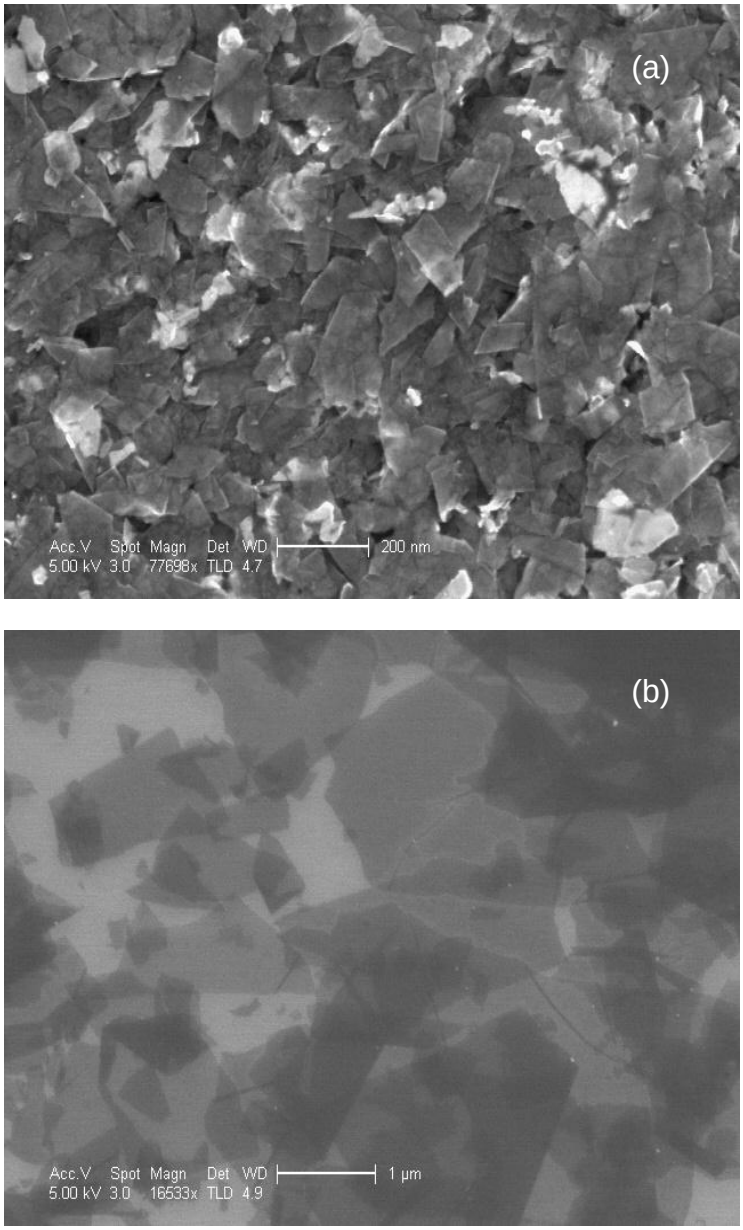

Figure 6.1: Top view SEM images revealing the grain sizes of (a) PCG films, (b) GO films deposited on SiO_2/Si substrate.

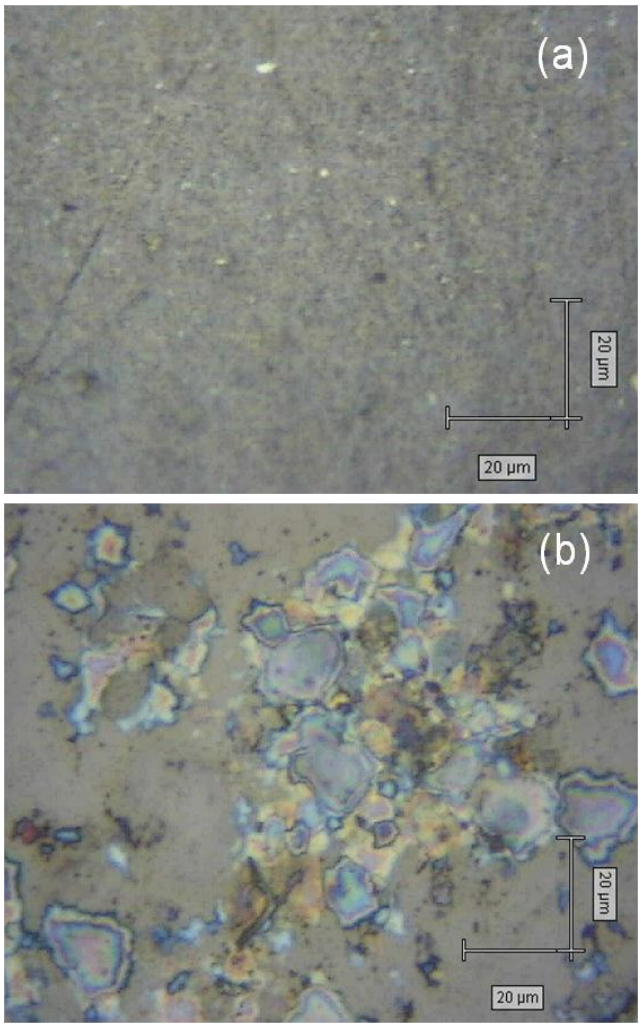

Figure 6.2: Optical microscopy images of (a) PCG and (b) GO films.

Figure 6.2 (a) and (b) shows the Raman spectra of both PCG and GO films respectively, investigated with the use of Renishaw Raman equipped with a 50x objective lens using an exciting source of 488 nm laser with spot size less than 1µm, recorded in

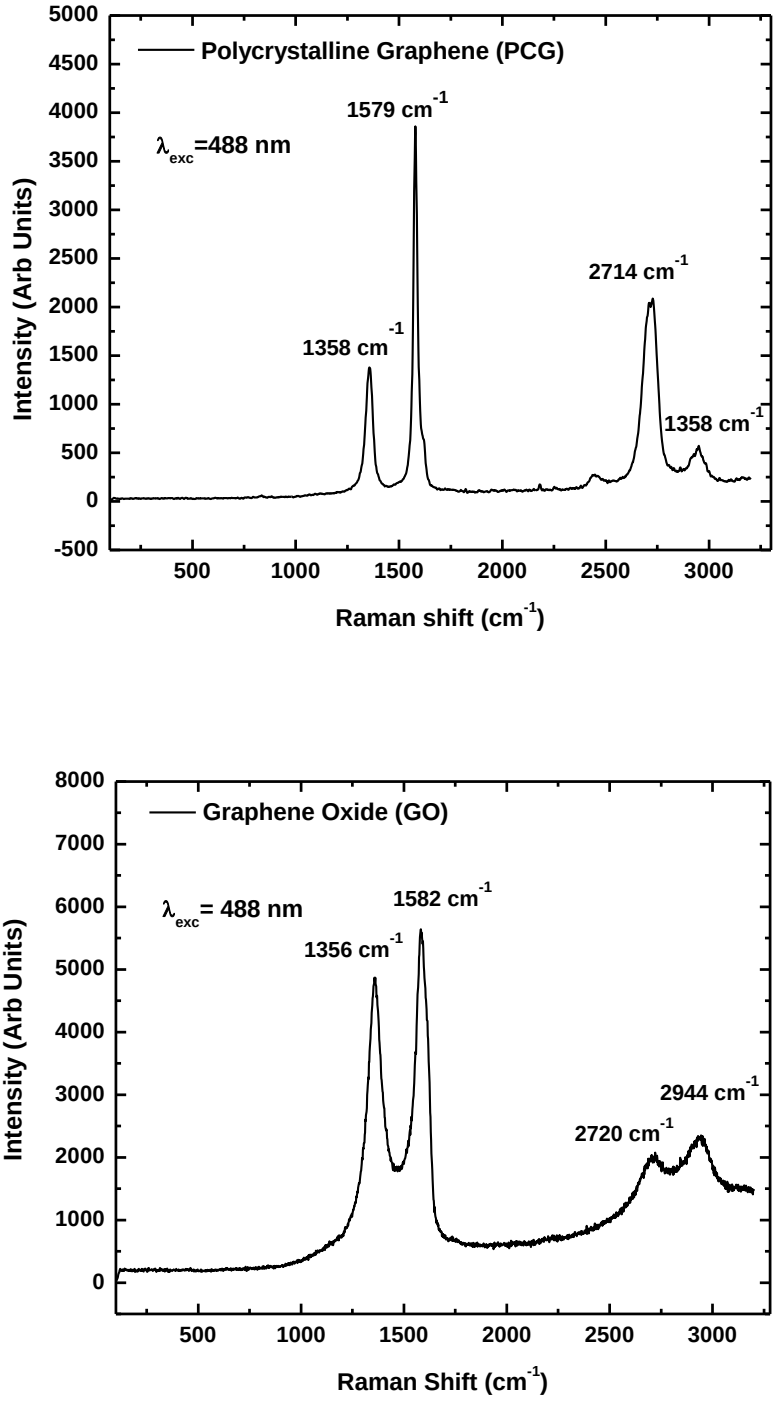

Figure 6.3: Raman spectrum of (a) PCG films (b) GO films.

backscattering configuration. Raman spectra of overlapped graphene flakes is similar to few layer (<5) graphene prepared by micromechanical cleavage. D and D' peaks are observed coming from the edges because of the small size of individual flakes (~200 nm). PCG has characteristic graphene Stokes *G* peak at 1579 cm^{-1} and a symmetric 2D peak at 2714 cm^{-1} which is nearly consistent with the reported SLG spectra [13]. In addition, PCG spectra also shows the disorder-*D* peak at 1358 cm^{-1}, which is expected for any polycrystalline material with degree of disorder and is consistent with that of small graphite crystallites [14]. GO has the Stokes *G* peak at 1582 cm^{-1}, 2D peak at 2720 cm^{-1} and the disorder *D* peak at 1356 cm^{-1}.

6.3 Thermal Conductivity Measurement of PCG and GO Films

Thermal conductivity measurements on PCG and GO films was performed using a non-contact optical technique based on micro-Raman spectroscopy, which was originally developed for the suspended single-layer graphene (SLG) flakes [3]. To use Raman technique for measurement of macro-sized PCG and GO films we designed a special sample holder to mimic the experimental set-up done for suspended graphene. Figure 6.4 shows the optical image of free standing PCG films suspended across the specially designed sample holder. A trench ~7 mm deep and 3mm wide was cut into the block and Aluminum pads were used as metal heat sinks. The films were stretched to avoid any folds and attached to the metal pads. Figure 6.4 shows that the dimensions of PCG/GO films investigated were on the order of ~3 mm in length and 2 mm in width, bridging the

two heat sinks. The surface of the sample holder was made abrasive to restrict any reflection of laser light. The schematic of the experimental setup has already been demonstrated by us earlier [3]. The interesting observation was that like graphene, PCG and GO also possess temperature sensitive signature *G* peak [15] which allowed us to measure the *G* peak temperature coefficient for these films and hence their thermal conductivity. It was performed by externally changing the temperature of PCG/GO films by placing them in the LINKAM TMS-94 temperature controller stage with platinum resistor sensor and focusing a constant laser light (488 nm) with low power level. Low power was used to reduce any heating effect of the specimen by the laser itself. However, measurements taken at low power produces high signal to noise (S/N) ratio, to improve S/N ratio we accumulated spectra from several spots and then averaged them. Proper hold time at each temperature was allowed for higher accuracy in measurements of temperature coefficients.

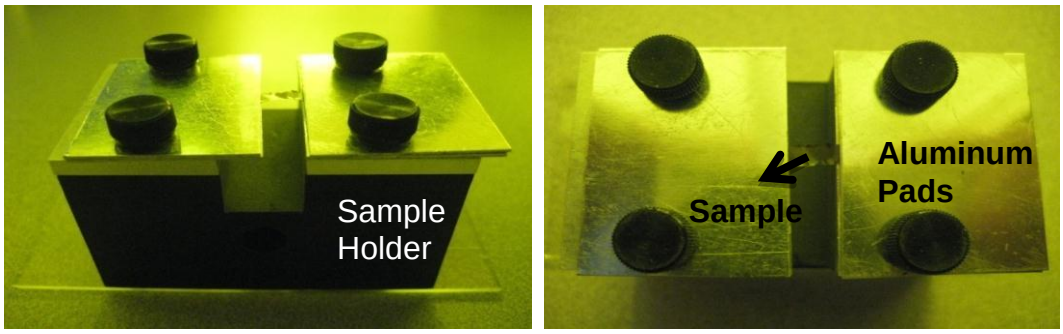

Figure 6.4: PCG and GO films suspended in sample holder designed for thermal conductivity measurements by optical Raman technique. Nano-Device Laboratory, UCR.

Figure 6.5 (a) and (b) shows the shifts in G peak position vs. temperature change for PCG and GO films respectively. The temperature coefficient can be deduced from the slope of the experimental data. G peak temperature coefficients for PCG was found to be -0.01096 and that for GO was found to be -0.04476. The data scatter for G peak for each T can be attributed to the sample non-uniformity and possible T drift during the measurement.

In order to calculate the thermal conductivity of these films, we also need to measure the shift in the G peak position due to the variation in the heating power on the surface. The power level at the PCG/RGO sample location was determined using an Ophir power meter calibrated with the standards traceable to the National Institute of Standards and Technology (NIST). The increase in the excitation power led to a red shift of the G peak for both PCG and GO films. This red shift indicates a rise in the temperature in the middle of the suspended PCG/GO. Figure 6.6 (a) and (b) shows the measured shift in G peak with increase in excitation power for PGG and GO respectively. The extracted slope $\Delta\omega/\Delta P$ was calculated as -0.894 cm^{-1}/mW for PCG and -1.074 cm^{-1} /mW for GO.

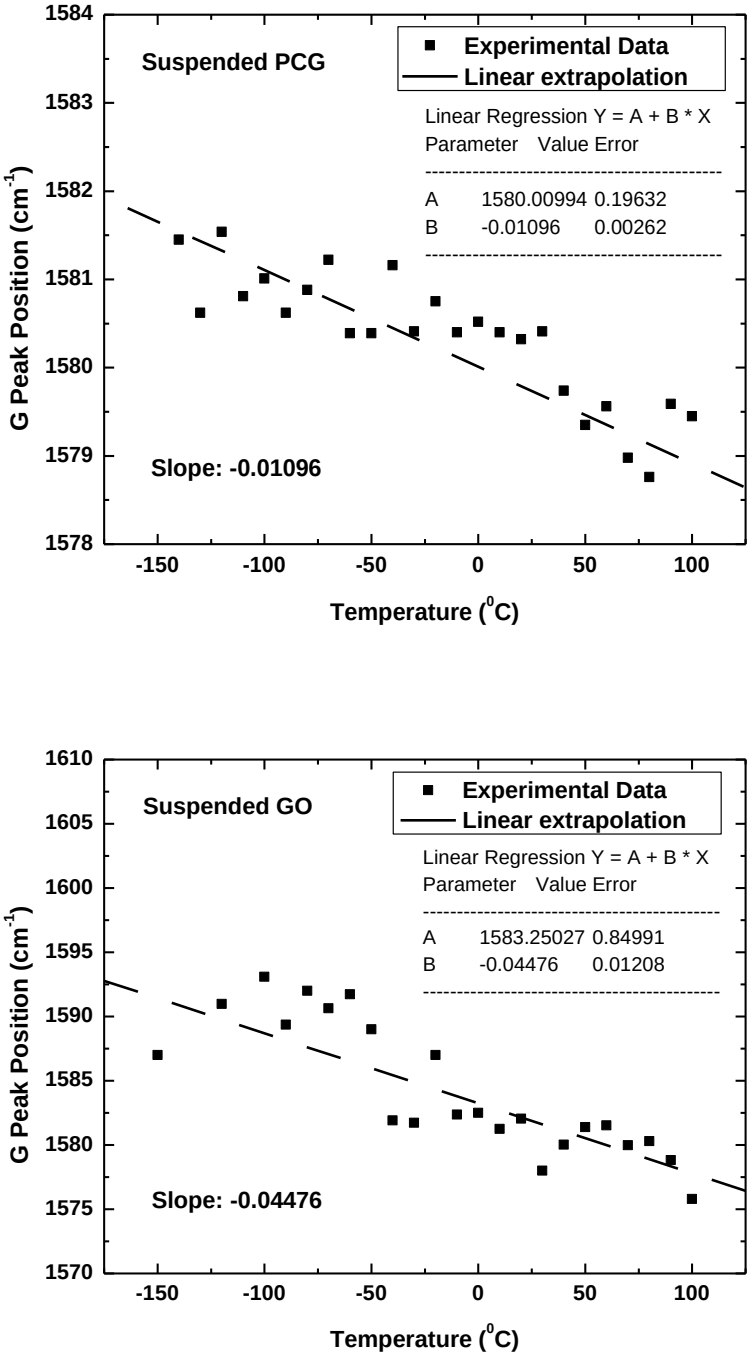

Figure 6.5: G-peak Raman shift as a function of temperature for free standing (a) PCG and (b) GO films.

The heat conduction equation derived for graphene [3] cannot be used for these films as these films are relatively very thick (on an order of several microns) as compared to single layer or bi-layer graphene. Here we need to study Gaussian distribution with spherical heat wave front in contrast to lateral heat flow assumed for graphene. We used finite element method (FEM) using COMSOL software [16] to solve the temperature distribution of polycrystalline graphene (PCG) and graphene oxide (GO) with their ends attached to the heat sinks. The temperature of the heat sink was maintained to be at room temperature (300K). Actual dimensions of PCG and GO were considered during the simulation runs to determine the thermal conductivity. In this case the heat dissipation to the air was ignored since air has negligible thermal conductivity (~0.024 $Wm^{-1}K^{-1}$). The heat conduction was modeled by numerically solving the Fourier's Law

$$-\nabla \cdot (k\nabla T) = Q \qquad [6.1]$$

where Q is the heat source, which is defined as the heat energy generated within a unit volume per unit time, T is the absolute temperature and k is the thermal conductivity. The temperature of the PCG/GO flake is locally increased in the middle with a laser source, considered to be a point source with Gaussian distribution. Since these were thick samples, as compared to single layer graphene, light cannot penetrate through the sample rather it will have spherical heat waves throughout the penetration depth. The excitation source distribution is given as

$$Q = P(x, y) = \frac{P_G}{\frac{2}{3}\pi R^3} \exp\left(-\frac{x^2 + y^2}{2\sigma^2}\right) \qquad [6.2]$$

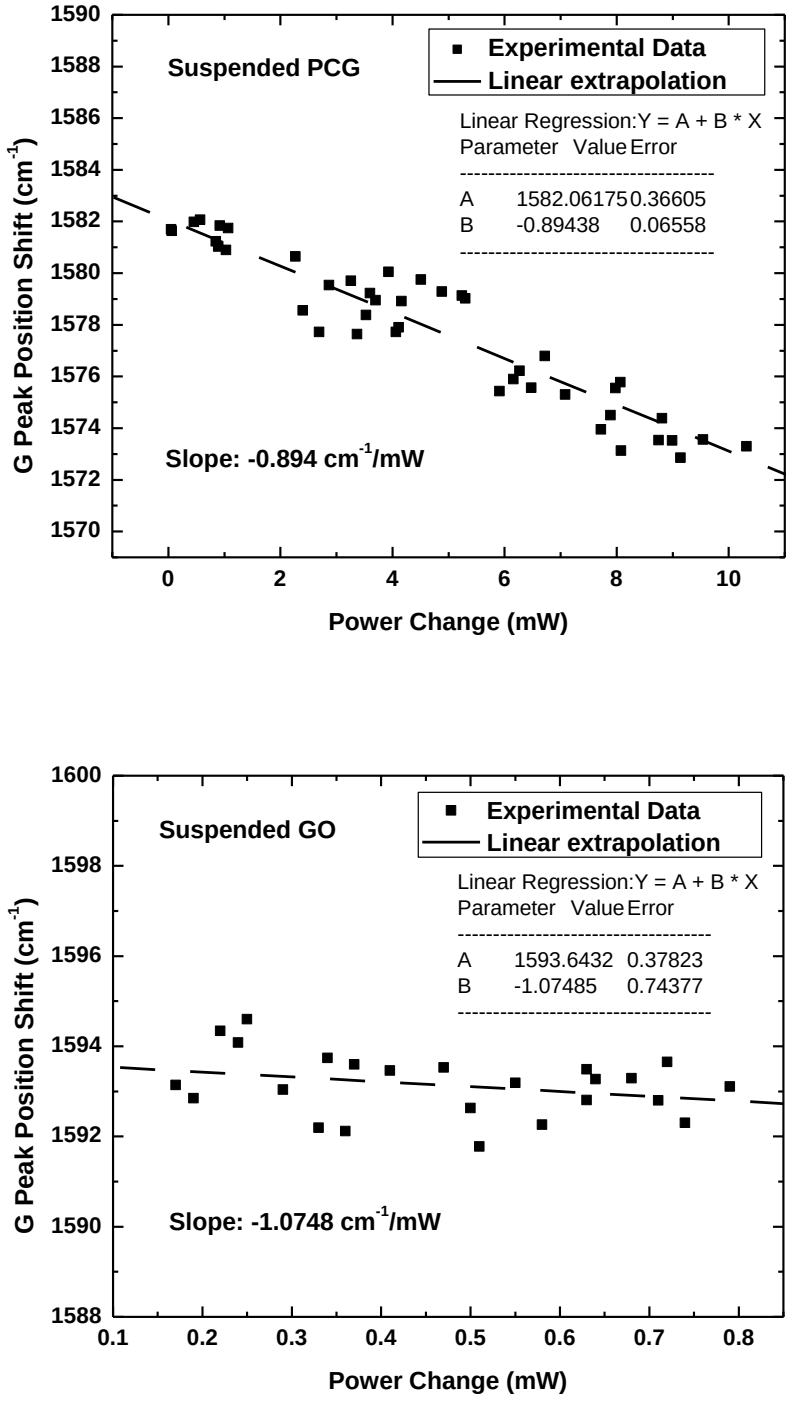

Figure 6.6: G-peak Raman shift as a function of induced laser power for free standing (a) PCG and (b) GO films.

The FWHM occurs at 0.5 μm which is the radius of our laser source. The two ends those are attached to heat sinks are specified as being kept at the room temperature. Figure 6.7 shows the schematic of the spherical heat wave front in PCG. All other boundaries are defined as being completely insulated from the surrounding environment,

$$\vec{n}.(k\nabla T) = 0 \qquad [6.3]$$

i.e., the temperature gradient across the boundary is considered zero. Figure 6.8 shows the temperature distribution in PCG simulated using COMSOL. During the simulations, both the power and experimentally extracted thermal conductivity are input parameters and the temperature distribution in the flake is a result of the simulation runs. The function

$$k = f(\theta) \qquad [6.4]$$

was studied to extract the thermal conductivity of PCG/GO flakes, where

$$\theta = \left(\frac{\partial \omega}{\partial P}\right) = \left(\chi \frac{\partial T}{\partial P}\right) \qquad [6.5]$$

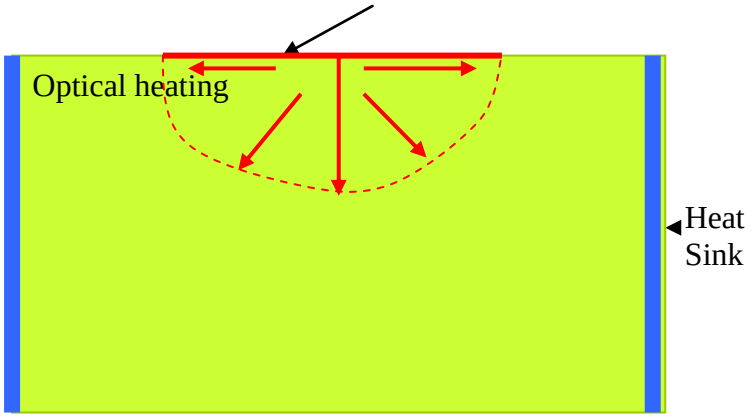

Figure 6.7: Schematic diagram showing spherical heat wave propagation in PCG

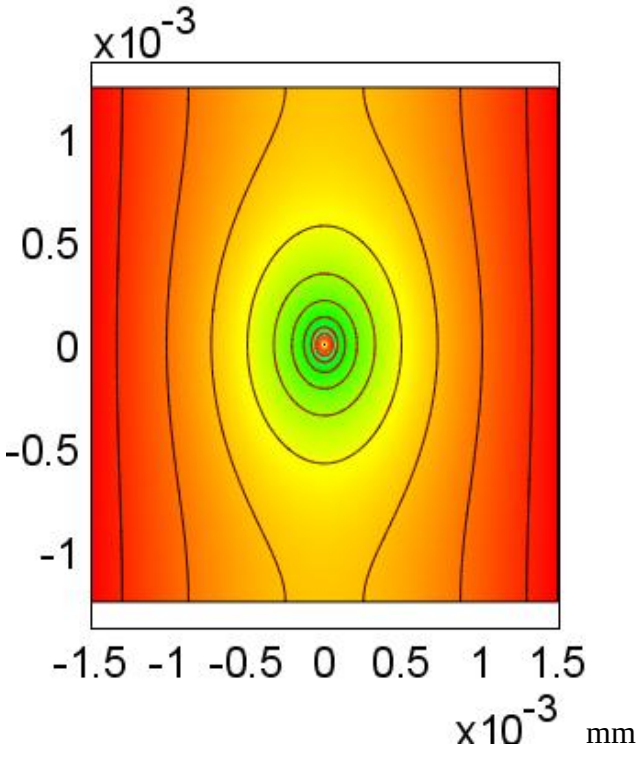

Figure 6.8: Temperature distribution in polycrystalline graphene sheet with K=45 W/mK with excitation power of 1.0mW considering 100% absorption in PCG. Simulation results are courtesy of Dr. Samia Subrina, Nano-Device Laboratory, UCR.

Figure 6.9 shows the thermal conductivity versus slope (cm^{-1}/W) curve from which, the thermal conductivity of PCG can be found. We estimated that the PCG exhibit thermal conductivity of ~45 W/mK and GO films exhibit thermal conductivity of ~124 W/mK. Flake to flake adhesion is more in the case of GO films than PCG which resulted in its higher thermal conductivity. The thermal conductivity of PCG/GO is quantitatively very low as compared to that of the suspended single-layer graphene (SLG) which is on the order of ~4000 W/mK. The latter is due to the fact that the mean-free-path (MFP) of phonons in SLG is limited by the graphene flake size rather than by Umklapp scattering. The thermal conductivity of PCG/GO films is dominated by phonon scattering at grain boundaries, structural defects and phonon – rough interface scattering (top and bottom surfaces). GO films exhibit higher thermal conductivity as compared to PCG owing to their bigger grain size [17].

To analyze our results, we studied electron dispersive spectra (EDS) of PCG films and studied the composition of the samples. It was found that along with the carbon, there was a significant ratio of oxygen present in the films which may have been introduced during the preparation, transfer, or oxidation from the atmosphere, etc. Figure 6.10 shows the EDS scan for PCG films showing composition of PCG: weight percent of carbon and Oxygen was measured to be ~85% and 14% respectively, with little fraction of Si. We calculated theoretically that the thermal conductivity of PCG films is dominated by scattering at the polycrystalline grain boundaries and structural defects caused y the presence of broken bonds and percentage of oxygen present in the films.

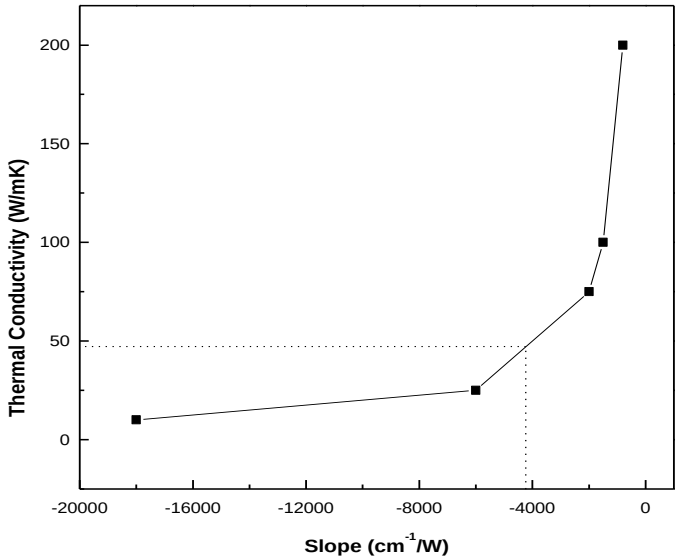

Figure 6.9: Thermal conductivity, K versus slope curve to extract thermal conductivity of PCG. Image is courtesy of Dr. Samia Subrina, Nano-Device Laboratory, UCR.

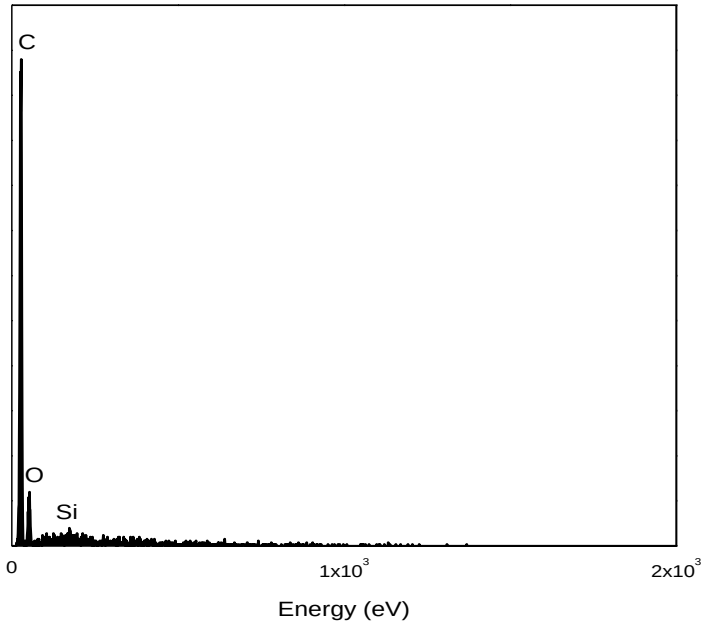

Figure 6.10: EDS spectra of PCG revealing its composition.

6.4 Electrical Characterization of PCG Films

Electrical properties of PCG were examined using a probe station (Signatone 4142) at ambient conditions. It is important to understand if the electrical conductivity of the PCG undergoes changes as compared to that of graphene for their proposal as interconnect material. The RT current-voltage characteristics shown in Figure 6.11 reveal linear I-V characteristics and reveal a sheet resistance of R_{sh} = 6.3 kΩ. It is noteworthy that the sheet resistance of PCG is in the range of already acceptable value for some applications [18].

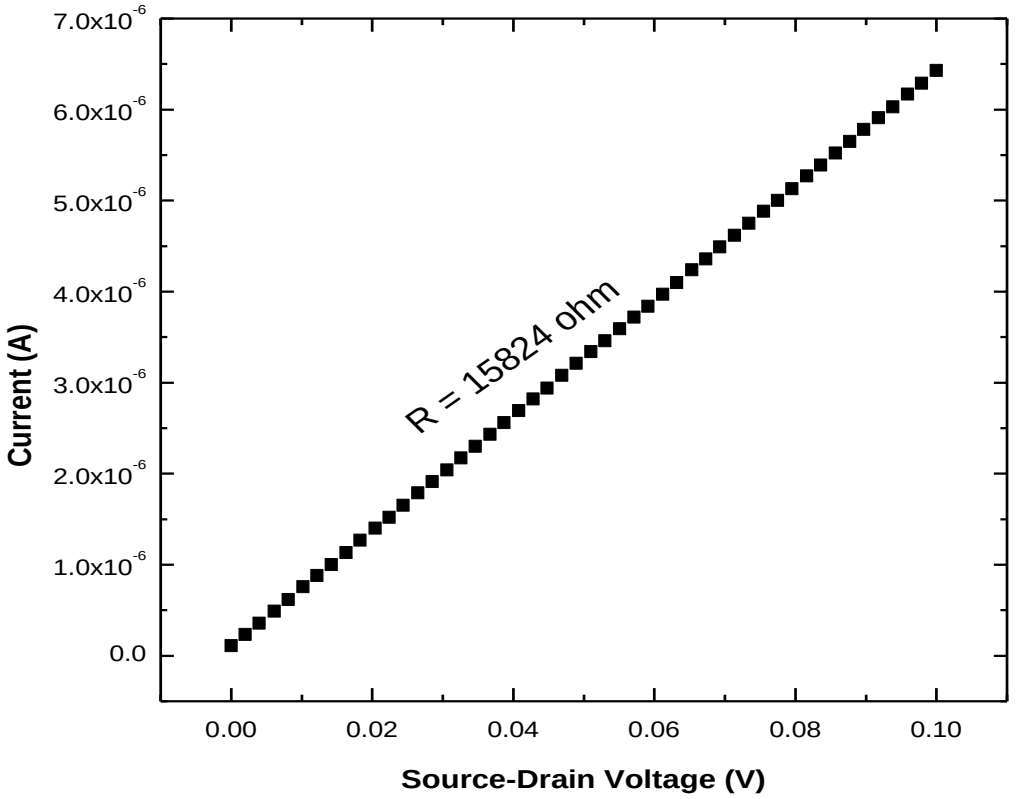

Figure 6.11: I-V characteristic of PCG with the 4-probe measurements.

6.5 Summary

In conclusion, we experimentally investigated the thermal conductivity of free standing polycrystalline graphene (PCG) and graphene oxide (GO) films. Thermal measurements on these films was done by using a combination of experiment using micro Raman optic technique which was originally developed for thermal conductivity measurements on single layer graphene (SLG) as well as simulation results using finite-element COMSOL multiphysics software. It was found that the thermal conductivity of PCG and GO films depends on the grain size and density of the flakes and is dominated by phonon scattering on polycrystalline grain boundaries and structural defects.

The thermal conductivity of the PCG/GO films is far less than that of SLG, but it is assumed to increase by increasing the grain size as well as the flake density, and they can outperform thin copper films and represent a less expensive and technologically feasible approach for applications in multi-layer interconnects wiring. In addition, Raman-based spectroscopy technique which was developed for thermal conductivity measurement of SLG was validated via direct power measurements for this experiment.

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Chapter 7

"Pseudo-Superlattices" of Bi_2Te_3 Topological Insulators

7.1 Introduction

Bismuth-telluride (Bi_2Te_3) has been a vital component of today's ever demanding thermoelectric industry since the discovery of its extraordinary thermoelectric properties in 1950's [1-3]. Bi_2Te_3 in its bulk form is known to have highest thermoelectric figure of merit, $ZT \sim 1.14$ at room temperature (RT). A high ZT thermoelectric material allows the direct conversion of thermal energy to electric energy that can be utilized without forming harmful byproducts*. The thermoelectric figure of merit is defined as

$$ZT=S^2\sigma T/K \qquad [7.1]$$

*Part of this chapter has been excerpted from V. Goyal, D. Teweldebrhan, and A.A. Balandin, "Mechanically-Exfoliated Stacks of Thin Films of Bismuth Telluride Topological Insulators with Enhanced Thermoelectric Performance," Appl. Phys. Lett. vol. 97, 133117, 2010. © 2010 American Institute of Physics; D. Teweldebrhan, V. Goyal and A. A. Balandin, "Exfoliation and Characterization of Bismuth Telluride Atomic Quintiples and Quasi-Two-Dimensional Crystals," Nano Lett. vol. 10, 1209, 2010 © 2010 Americal Chemical Society; D. Teweldebrhan, V. Goyal, M. Rahman and A. A. Balandin, "Atomically Thin Crystalline Films and Ribbons of Bismuth Telluride," Appl. Phys. Lett. vol. 97, 133117, 2010. © 2010 American Institute of Physics.

where, $S=-\Delta V/\Delta T$ is the Seebeck coefficient, ΔV is the voltage difference corresponding to a given temperature difference ΔT, σ is the electrical conductivity and K is the thermal conductivity, which has contributions from electrons and phonons. It is clear from ZT definition that in order to improve thermoelectric figure of merit one should increase the thermopower $S^2\sigma$ and decrease the thermal conductivity. Different approaches have been tried in order to enhance the thermoelectric properties of Bi_2Te_3 or its alloys. These approaches included the composition change from its stoichiometry, the use of polycrystalline materials with different grain sizes, intentional introduction of structural defects and incorporation of different dopants, e.g. Sb or Se, into Bi_2Te_3 lattice. The optimization of bulk Bi_2Te_3 led to incremental improvements but no breakthrough enhancement in ZT was achieved. For example, p-type 100 nm/500 nm Bi_2Te_3/Sb_2Te_3 and n-type 100 nm/500 nm $Bi_2Te_3/Bi_2Te_{2.83}Se_{0.17}$ superlattice structures have theoretically been predicted of achieving significantly higher room temperature figure of merit values as high as ~2.34 and ~1.46, respectively [3]. Recent it has been indicated that the low-dimensional structuring of BiSbTe alloys [4] also allows for ZT enhancement up to ~1.5 at RT. But still higher ZT values are needed for a major practical impact. It has been shown that ZT above 3 or 4 at RT are needed in order to make thermoelectric cooling or power generation competitive with conventional methods [5]. Such an increase in ZT would lead to a "thermoelectric revolution" and allow one for much more environmentally friendly power generation and cooling.

A great deal of effort has been devoted to increase ZT of Bi_2Te_3 based materials. It has been predicted theoretically that a drastic improvement in ZT can be achieved in

low-dimensional structures where electrons (holes) are strongly confinement in one or two dimensions [6]. Hicks and Dresselhaus [7] predicted that *ZT* can be increased in Bi_2Te_3 quantum well by a factor of ~13 over the bulk value. The crucial condition for such ZT enhancement is a complete carrier confinement in a quantum well with a width *H* on the order of ~1 nm and an optimized position of the Fermi level. This can only be possible if materials are crystalline and essentially free of defects. According to Dresselhaus *et al*. [6-7], quantum confinement of charge carriers in quantum wells leads to a drastic *ZT* improvement due to the increase in the carrier density-of-states (DOS) near the Fermi level and corresponding increase in the thermopower $S^2\sigma$. The thickness of the thin film required to achieve the quantum confinement conditions has to be on the order of few atomic layers. It is important to note here that in the Bi_2Te_3 based superlattices which are commonly used in thermoelectric studies, the charge carries are only partially confined due to the small potential barrier height and relatively low material quality. Conventional chemical vapor deposition, molecular beam epitaxy (MBE), electrochemical or other means are not capable for producing such quality structures. The barrier height has a pronounced effect on *ZT*. Broido and Reinecke [8] have shown theoretically that a ZT=3 can be achieved in Bi_2Te_3 superlattices with infinite potentials when the quantum well width (i.e. thickness of the thin film) is H~3 nm. In the structures with incomplete quantum confinement the maximum *ZT* decreases to ~2.5 and the required width becomes as small as ~2 nm.

In another theoretical approach, Balandin and Wang [9-10] proposed a different strategy for increasing *ZT* in low-dimensional structures by reducing its thermal

conductivity via spatial confinement of acoustic phonons, which carry bulk of heat in thermoelectric materials. This thermal conductivity reduction originates from the decreased phonon group velocity of the confined acoustic phonon modes, which results in the increased scattering at point defects [9-11]. Nanostructured materials, such as superlattices, can have drastically reduced thermal conductivity in comparison to the corresponding bulk values, which results from the phonon scattering on boundaries and defects [12-13]. Thus superlattices have become promising candidates in search for high-efficiency thermoelectric devices [3, 7-10, 12]. Thus, in order to employ the full strength of the low-dimensional confinement effects for improving thermoelectric figure of merit either via the electron band-structure and phonon engineering one needs to produce quasi-two-dimensional (2D) structures with a few-atomic layer thickness and high quality interfaces. These considerations create very strong motivations for the search of alternative approaches to fabrication of the stacks of quasi-2D crystals made of Bi_3Te_3-based materials.

Most recently, the interest to the stacked quasi-2D layers of bismuth telluride received an additional impetus from a new direction. It has been shown that stacks of quasi-2D layers of Te-Bi-Te-Bi-Te are members of a new type of recently discovered materials referred to as topological insulators [14-16]. TIs are materials with a bulk insulating gap and conducting surface states that are topologically protected against scattering by the time-reversal symmetry [14]. The surface state of a quasi-2D crystal of Bi_2Te_3 is predicted to consist of a single Dirac cone. Moreover, it has been shown that the layered structures of related materials such as Bi_2Se_3 and Sb_2Te_3 are also topological

insulators. The particles in topological insulators coated with thin ferromagnetic layers have manifested exotic physics and were proposed for possible applications in the magnetic memory where write and read operations are achieved by purely electric means. It was shown theoretically that *ZT* can be strongly enhanced in Bi_2Te_3 thin-film TIs provided that the Fermi level is tuned to ensure the surface transport regime and the films are thin enough to open a gap in the "Dirac cone" dispersion on the surface [17-18]. All these stimulate the search for methods to produce stacks of quasi-2D crystals of bismuth telluride even further.

In this chapter, we report on thermoelectric properties of "pseudo-superlattices" prepared by staking of the "graphene-like" mechanically exfoliated single-crystal Bi_2Te_3 films. The thermal conductivity reduction (both the in-plane and the cross-plane) with preserved electrical properties leads to strong increase in the thermoelectric figure of merit of these stacked structures [19]. This technique will open up a new strategy since Bi_2Te_3 and related alloys are shown to be topological insulators. This fabrication technique can further be extended to other thermoelectric materials of the bismuth telluride family, e.g. Bi_2Se_3, Sb_2Te_3, etc.

7.2 Sample Preparation and Characterization

Bi_2Te_3 has a layered structure as shown in Figure 7.1. Its atomic arrangement can be visualized in terms of the layered sandwich structure where each sandwich is built up by five mono-atomic sheets referred to as *quintuple* layers. The atomic planes follow the

sequence $Te^{(1)}$-Bi-$Te^{(2)}$-Bi-$Te^{(1)}$, which is then repeated. The superscripts are used to distinguish two types of differently bonded tellurium atoms. The $Te^{(1)}$-$Te^{(1)}$ layers are held together by weak van der Waals forces, while the remaining atoms are linked by strong ionic-covalent bonds [20]. The bond strength within the quintuple layers is not the same. The Bi-$Te^{(1)}$ bond is stronger than Bi-$Te^{(2)}$ bond, which is the second weakest points within the crystal structure.

It is believed that the Bi-$Te^{(2)}$ bond is covalent while the Bi-$Te^{(1)}$ binding includes both covalent and ionic interaction. Single crystals of bismuth telluride can be cleaved readily in the plane of the *a*-axes. The lattice spacing between layers has a direct relationship with the atomic bond strength between the neighboring layers. For this reason the weakest $Te^{(1)}$-$Te^{(1)}$ bond correspond to the largest spacing d~0.37 nm. What is also important for our purposes is that the strength and length of Bi-$Te^{(2)}$ bond is not much different from the van der Waals gaps of $Te^{(1)}$-$Te^{(1)}$. The latter suggests that the mechanical exfoliation may lead not only to [$Te^{(1)}$-Bi-$Te^{(2)}$-Bi-$Te^{(1)}$] quintuples but also to separate atomic planes of Bi-Te and Te-Bi-Te.

We previously demonstrated that a "*graphene-like*" mechanical exfoliation procedure can be used to mechanically exfoliate the ultra-thin films of Bi_2Te_3 with the thickness down to a single *quintuple* [21-22]. The mechanically exfoliated few-quintuple films have a number of benefits compared to grown thin films. They are perfectly crystalline and have an essentially infinite potential barrier for electrons and holes.

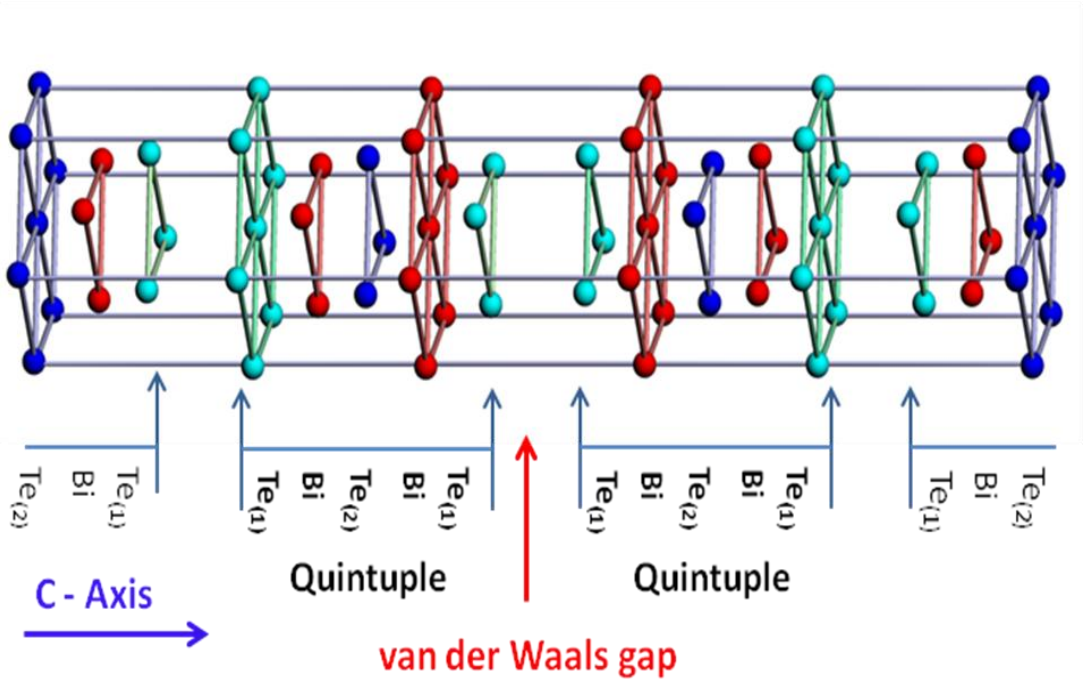

Figure 7.1: Schematic of Bi_2Te_3 crystal structure. The $Te^{(1)}$-$Te^{(1)}$ bond is the weakest while Bi-$Te^{(1)}$ bond is the strongest. Reprinted with permission from D. Teweldebrhan, V. Goyal and A. A. Balandin, "Exfoliation and Characterization of Bismuth Telluride Atomic Quintiples and Quasi-Two-Dimensional Crystals," *Nano Lett* vol. 10, 1209, 2010 © 2010 Americal Chemical Society.

The latter is a drastic difference from Bi_2Te_3-based superlattices grown by molecular beam epitaxy (MBE), metal-organic chemical vapor deposition (MOCVD), or other techniques. The ultimately high potential barriers together with a few-quintuple thickness and possibility of electrical back-gating can ensure the strong quantum confinement for electrons and E_F fine-tuning which can result in tremendous increase in *ZT* figure of merit as suggested theoretically [6-7, 9-10]. At the same time, the thermoelectric applications require a sufficient quantity of material, i.e. "bulk", i.e. the

single quintuples would hardly be practical. For this reason, we studied the stacks of the exfoliated films, which were put on top of each other and subjected to thermal treatment. Figure 7.2 shows the scanning electron microscopy image of two overlapping mechanically exfoliated films.

The "*graphene-like*" exfoliated Bi_2Te_3 thin films with different thicknesses (ranging from few nm to μm) were transferred to a substrate and mechanically put on top of each other to form a stack. These stacks were then annealed at ~250 ^{0}C for 30 second to reduce the air gaps between the layers and improve structural stability. Figure 7.3 shows the cross-sectional scanning electron microscopy (SEM) image (Philips XL-30 FEG) of a stacked sample.

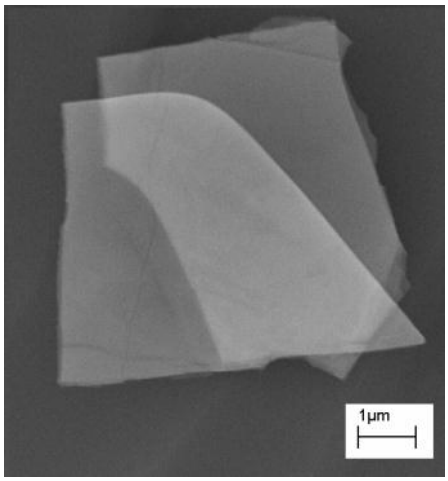

Figure 7.2: Scanning electron microscopy (SEM) image of two overlapping mechanically exfoliated films. Reprinted with permission from V. Goyal, D. Teweldebrhan, and A.A. Balandin, "Mechanically-Exfoliated Stacks of Thin Films of Bismuth Telluride Topological Insulators with Enhanced Thermoelectric Performance," *Appl. Phys. Lett*. vol. 97, 133117, 2010 © 2010 American Institute of Physics.

The non-periodic "superlattices" may have certain benefits for thermoelectric applications owing to flexibility for tuning the phonon transport [23-24]. The stacks were intentionally made rather thick (up to ~0.5 mm). Indeed, for reducing the thermal conductivity along the cross-plane axis, it might be useful to intentionally introduce some disorder by making the layer thickness have a degree of randomness. Such randomness would induce Anderson localization of the phonons [25].

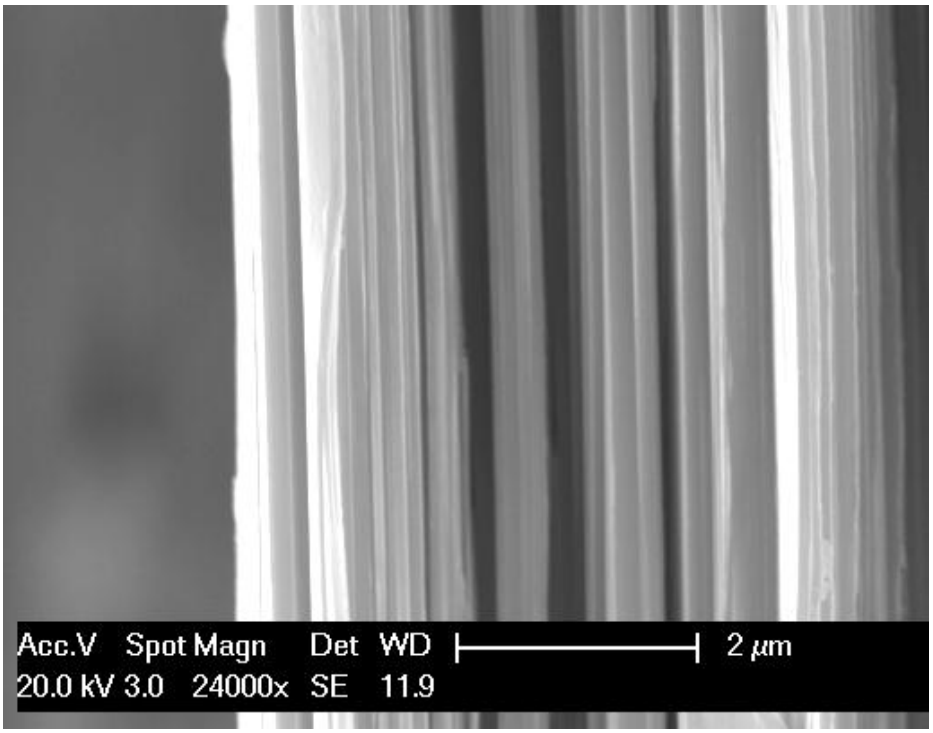

Figure 7.3: Cross-sectional SEM image of the stacked "pseudo-superlattice" of the mechanically exfoliated Bi_2Te_3 films. Reprinted with permission from V. Goyal, D. Teweldebrhan, and A.A. Balandin, "Mechanically-Exfoliated Stacks of Thin Films of Bismuth Telluride Topological Insulators with Enhanced Thermoelectric Performance," *Appl. Phys. Lett*. vol. 97, 133117, 2010 © 2010 American Institute of Physics.

The material crystallinity and quality were verified with micro-Raman spectroscopy (Renishaw RM 2000) used in a backscattering configuration. Figure 7.4 shows a spectrum of the exfoliated Bi_2Te_3 film recorded under 488-nm laser excitation. The observed peaks, $E_g^1(TO)$, $A^1_{1g}(LO)$, $E_g^2(TO)$, and $A^2_{1g}(LO)$, are consistent with literature for crystalline Bi_2Te_3 [26]. An additional peak, identified as A_{1u}, also appears for our exfoliated films, which appears as a result of the crystal symmetry breaking in thin films with the thickness below the light penetration depth [27] and is not present in the bulk Bi_2Te_3 crystals. The intensity if A_{1u} peak and the intensity ratio $I(A_{1g}^2)/I(E_g^2)$ can be used for nanometrology of few-quintuple films [26]. The shown spectra correspond to the film with the thickness W~50 nm. The thickness was cross-checked with the atomic force microscopy.

The diffraction pattern of the layers was studied using transmission electron microscopy (TEM). The sample preparation for TEM (FEI-PHILIPS CM300) characterization was carried out through ultrasonic separation in ethanol (C_2H_5OH) solution. The sonication was done with 500 µL of C_2H_5OH solution where the molar concentration of Bi-Te films was held at a constant 1.41 x 10^{-1} moles/liter throughout the solution. Figure 7.5 shows an electron diffraction pattern indicating the individual exfoliated films are crystalline. The films elemental composition and stoichiometry were studied with the energy dispersive spectroscopy (EDS). The presence of prominent Si and O peaks indicates that the individual films constituting pseudo-superlattices are transparent to the electron beams (see Figure 7.6).

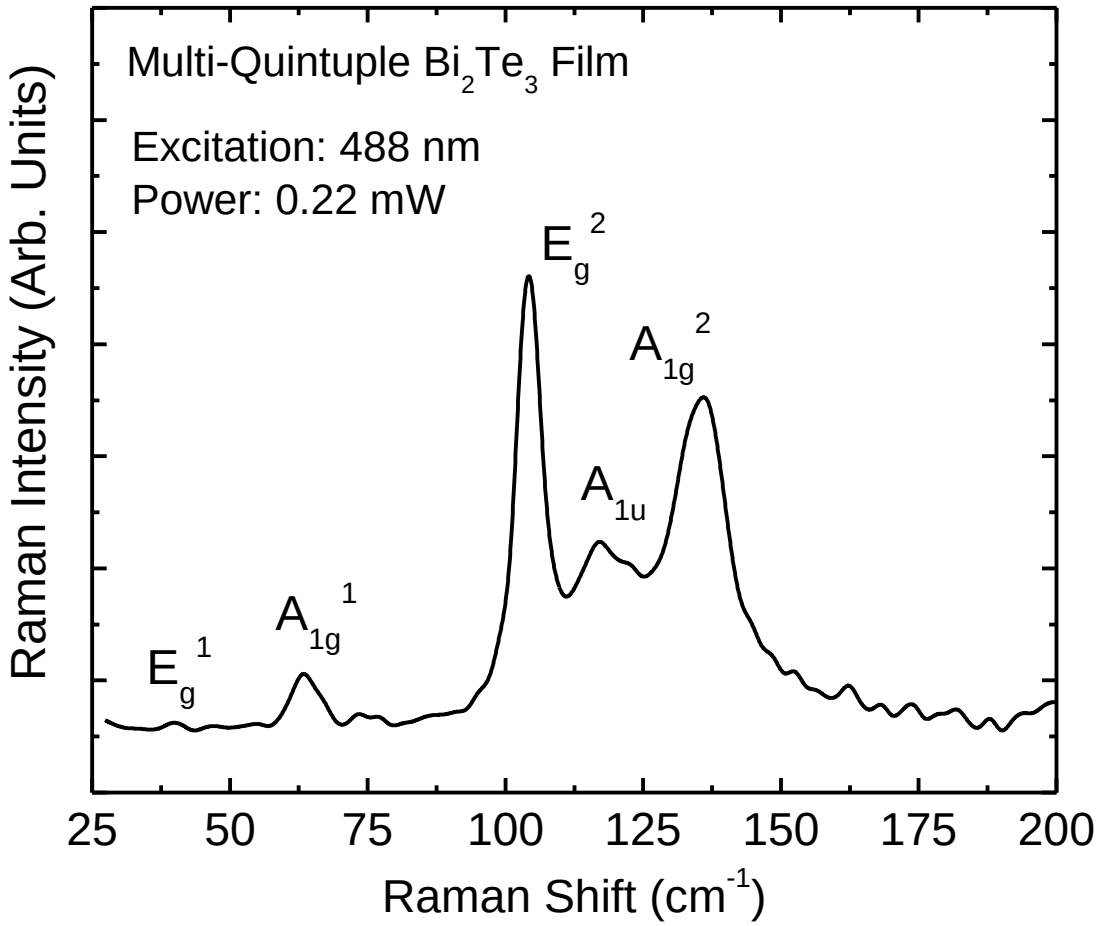

Figure 7.4: Raman spectrum of the "graphene-like" exfoliated Bi_2Te_3 films. Note the appearance of A_{1u} peak, not Raman active in bulk crystals, due to the crystal symmetry breaking in thin films. Reprinted with permission from V. Goyal, D. Teweldebrhan, and A.A. Balandin, "Mechanically-Exfoliated Stacks of Thin Films of Bismuth Telluride Topological Insulators with Enhanced Thermoelectric Performance," *Appl. Phys. Lett*. vol. 97, 133117, 2010 © 2010 American Institute of Physics.

Figure 7.5: Electron diffraction pattern of individual exfoliated Bi_2Te_3 film indicating crystallinity of the films.

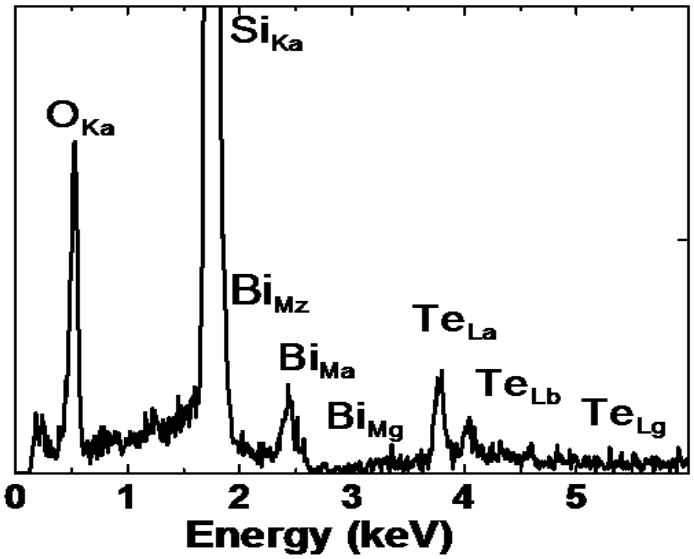

Figure 7.6: EDS spectrum of the exfoliated films indicating their atomic composition and transparency for the electron beam. Reprinted with permission from V. Goyal, D. Teweldebrhan, and A.A. Balandin, "Mechanically-Exfoliated Stacks of Thin Films of Bismuth Telluride Topological Insulators with Enhanced Thermoelectric Performance," *Appl. Phys. Lett*. vol. 97, 133117, 2010 © 2010 American Institute of Physics.

7.3 Thermal Conductivity of Mechanically-Exfoliated Bi_2Te_3 "Pseudo-Superlattices"

A superlattice is anisotropic, with a different thermal conductivity along the layers, i.e., in-plane and in the cross-plane direction. The experiments and the theories for these two directions are very different. The measurements of the thermal conductivity, *K*, on our stacked samples were performed by two different experimental techniques to obtain its in-plane and cross-plane components. The first technique was the transient plane source (TPS) "hot disk" technique (described in detail in Ch.3) which measures the average in-plane thermal conductivity. The second technique was the optical "laser flash" technique (LFT), which measures the average cross-plane *K*. In TPS technique [28], an electrically insulated sensor is sandwiched between two pieces of the sample under investigation. During measurement, a short electric pulse is passed through the sensor, which generates heat. The sensor acts both as a heat source and a thermometer to determine the temperature rise, ΔT, in the sample as a function of time, which is used to determine the thermal diffusivity, and specific heat, required for determining *K* value. Our LFT instrument (Netzsch NanoFlash LFA 447) is equipped with a xenon flash lamp which heated the sample from one end by light shots. The temperature rise (upto 2K) was determined at the back side of the samples with the nitrogen-cooled InSb IR detector. Using the thermal-wave travel time, we determined *K* from the equation $K=\alpha\rho C_p$, where C_p is the heat capacity and ρ is the mass density of the material and α is the thermal diffusivity of the film determined in the experiment as $\alpha = 0.139\times Z^2/t_{1/2}$, $t_{1/2}$ is the measured half-rise time of temperature [29-30]. Due to the geometry of the setup the

measured *K* has to be interpreted as mostly cross-plane component of the thermal conductivity tensor.

Figure 7.7 presents the results of our thermal measurements for three representative "pseudo-superlattices" with thicknesses ~0.4 mm, ~0.3 mm and with ~0.1 mm, reference bulk samples, and literature data for bulk Bi_2Te_3. A comparison with *K* values for Bi_2Te_3 from literature [31] indicates an excellent agreement and attests to the accuracy of our measurements. The monotonic *K* decrease with *T* is characteristic for semiconductor materials where thermal transport is limited by the crystal inharmonicity. The data for the bulk cross-plane *K* are also consistent. A strong decrease in both the in-plane as well as cross-plane thermal conductivity of the "pseudo-superlattices" was observed as compared to the bulk (see Figure 7.6). The in-plane *K* for the stacked Bi_2Te_3 superlattices is ~0.7 W/mK, which is a reduction by a factor of ~2.4 from the bulk value of ~1.7 W/mK. The RT cross-plane *K* of the stacked films is ~0.14 W/mK, which is a significant drop, by a factor of 3.5, from the bulk cross-plane value of ~0.5 W/mK. The "pseudo-superlattice" *K* is only weakly dependent on temperature which can be attributed to the thermal transport limited by the phonon – boundary scattering [9-10, 32-33]. The thermal conduction in our samples was mostly by the acoustic phonons; the electron contribution was estimated to be ~10% as calculated from the Wiedemann-Franz law.

Another interesting observation is that the *K* values obtained for the stacks with different thicknesses are nearly the same indicating that the thermal conductivity was limited by the phonon scattering at the interfaces between the individual Bi_2Te_3 layers

rather than by the scattering on the outside boundaries of the samples. The overall decrease of *K* in our stacks is exceptional. It is on the higher of that reported for Bi_2Te_3 nanoparticles [33], alloy films [34] and highly-textured materials [35]. The cross-plane *K* reduction is much stronger possibly owing to the large thermal boundary resistance between the exfoliated films. The cross-plane *K* in our "pseudo-superlattices" approaches the theoretical minimum value predicted for the disordered crystals [36].

The Seebeck coefficient of stacked films was determined using MMR system (SB100) consisting of two pairs of thermocouples. One pair was formed with the junctions of copper and a reference material (constantan wire with the known Seebeck coefficient of ~36μV/K). The other pair was formed with the junctions of copper and the layers under test. We modified the sample stage of the system in order to be able to use it with our thin films. The computer controlled sample stage was attached to the cold stage refrigerator and provides a pre-set stable temperature during the measurement. The sample chamber was kept at pressure below 10mTorr while in operation. The Seebeck measurements gave *S* values in the range of ~231-247 μV/K. The higher values were obtained for thinner samples.

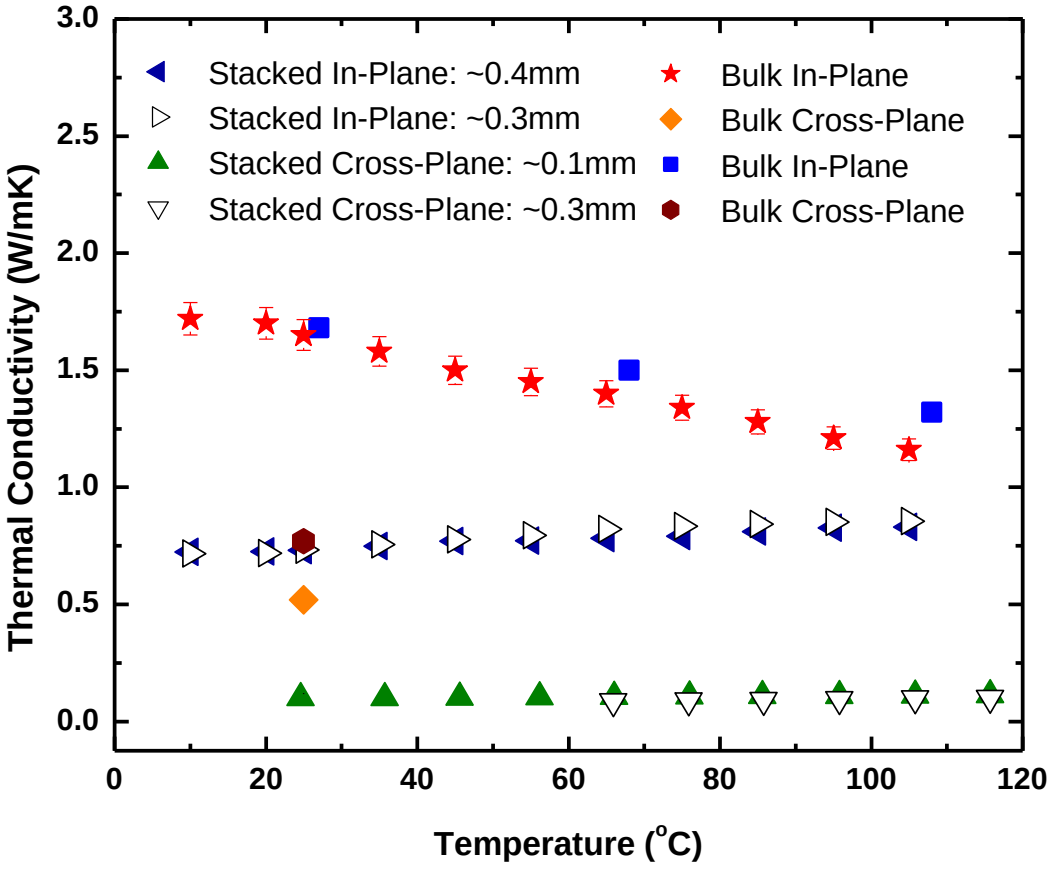

Figure 7.7: Thermal conductivity as a function of temperature for the stacked "pseudo-superlattices" and reference bulk Bi_2Te_3 crystals. The literature values for bulk Bi_2Te_3 are also shown for comparison. Reprinted with permission from V. Goyal, D. Teweldebrhan, and A.A. Balandin, "Mechanically-Exfoliated Stacks of Thin Films of Bismuth Telluride Topological Insulators with Enhanced Thermoelectric Performance," *Appl. Phys. Lett.* vol. 97, 133117, 2010 © 2010 American Institute of Physics.

The current – voltage characteristics of the "pseudo-superlattices" with different thicknesses were studied using probe station (Signatone and HP4142) at ambient conditions (see Figure 7.8). The electrical measurements revealed electrical resistivity on the order of ~10^{-4} Ωm, which is close to the optimum for the thermoelectric applications.

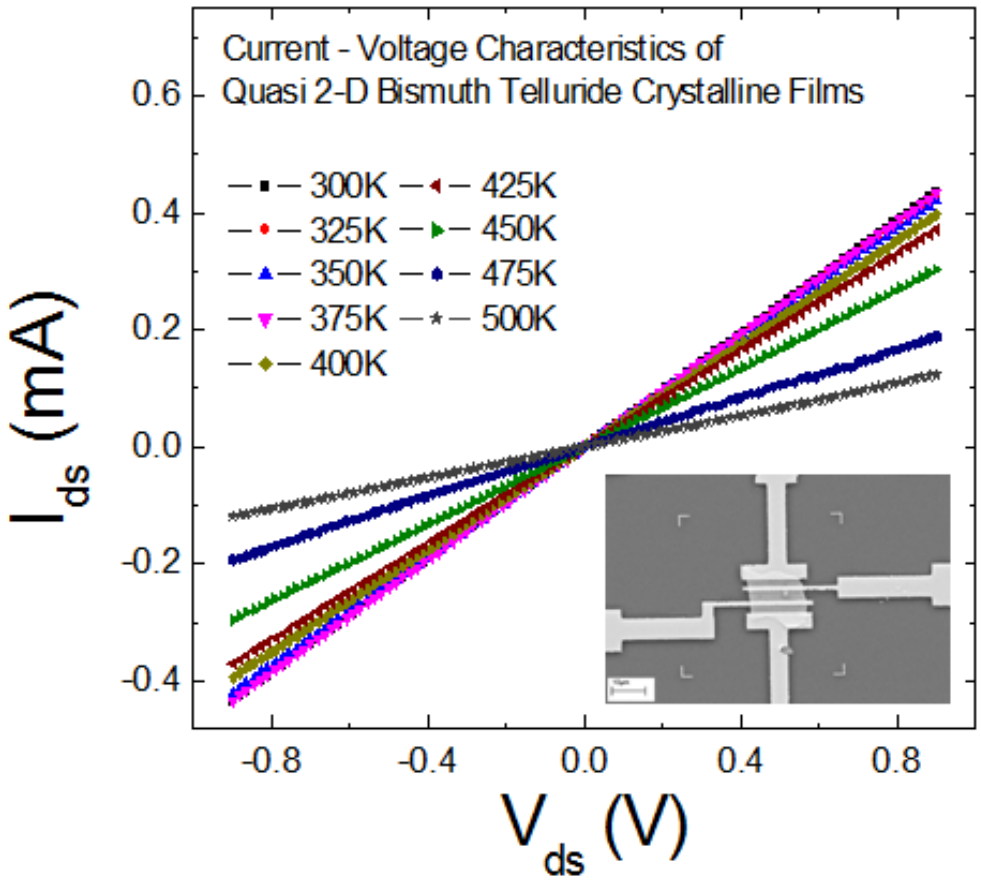

Figure 7.8: Current-voltage characteristics of stacked Bi-Te samples in the low bias region for different temperature. Reprinted with permission from D. Teweldebrhan, V. Goyal, M. Rahman, and A.A. Balandin, "Atomically-thin Crystalline Films and Ribbons of Bismuth Telluride," *Appl. Phys. Lett*. vol. 96, 053107, 2010 © 2010 American Institute of Physics. Inset image is courtesy of M.Z. Hossain, Nano-Device Laboratory, UCR.

The strong decrease in the thermal conductivity with preserved electrical properties translates to ~140-250% increase in *ZT* at RT. The estimated ZT enhancement is achieved entirely via reduction in the thermal conductivity. This enhancement can further be increased by increasing their crystal quality, thinning of the films and gating (for achieving the pure surface transport) [17-18].

7.4 Annealing Effect on the Thermal Conductivity of Bi-Te stacked 'Pseudo-Superlattices'

We intensively analyzed the effect of annealing on *K* of these 'pseudo-superlattices'. Annealing at 350^{o}C for 30 seconds led to ~5% increase in the thermal conductivity at RT. The latter was attributed to stronger bonds between the exfoliated Bi_2Te_3 layers and further decrease in the air gaps. The annealing at 450^{o}C for the same time led to the approximately the same decrease in *K* [19]. Figure 7.9 shows the in-plane thermal conductivity of stacked samples as a function of temperature with different annealing temperatures (for a sample of 0.3mm thickness).

This can be explained by the on-set of inter-diffusion between the layers and increased disorder. The latter was confirmed by the cross-plane SEM studies. The melting point for Bi_2Te_3 is rather low (T_m~570^{o}C), which supports our conclusion. The annealing temperature and time were optimized by hit and trial to enhance the adhesion of the exfoliated films to each other without damaging the pseudo-superlattice design by inter-diffusing of the films into each other. Figure 7.10 shows cross-sectional SEM

(Philips XL-30 FEG) image of stacked pseudo superlattices of exfoliated Bi_2Te_3 films (a) before and (b) after annealing. It is clear from the SEM images that the air gaps have been reduced and the structure has been stabilized as a result of annealing; and this explains the *K* dependence on annealing temperature [37].

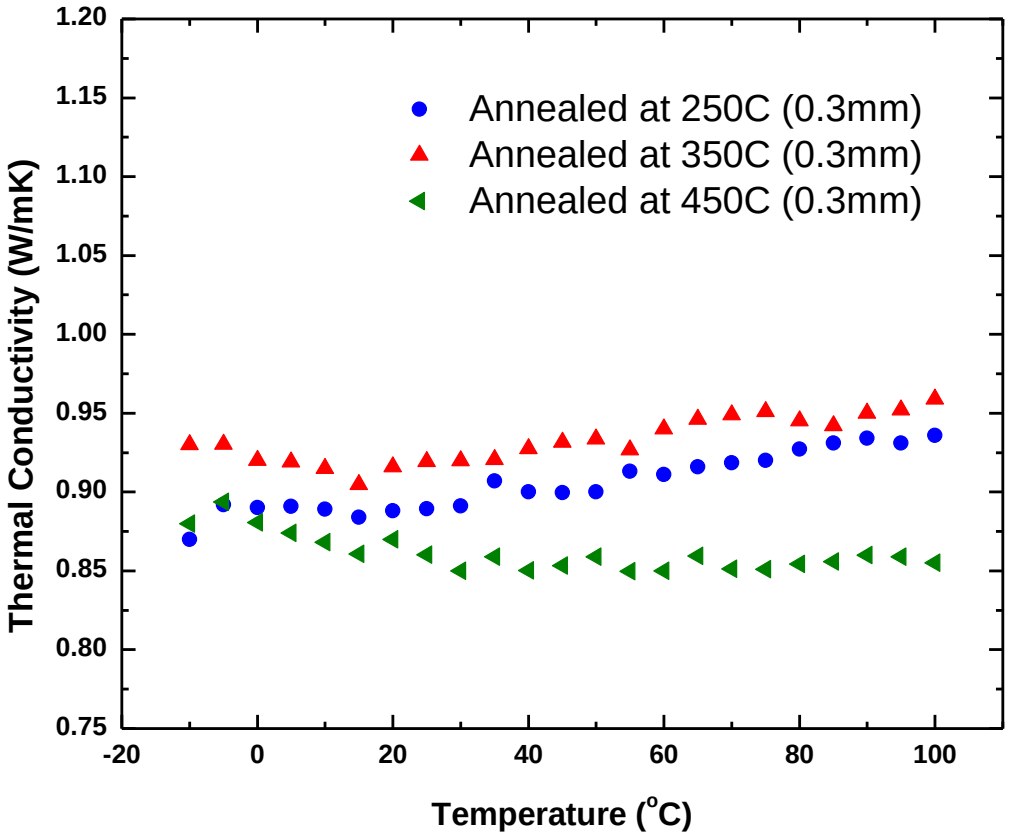

Figure 7.9: In-plane thermal conductivity as a function of temperature with different annealing temperatures for stacked "pseudo-superlattice" with ~0.3 mm thickness.

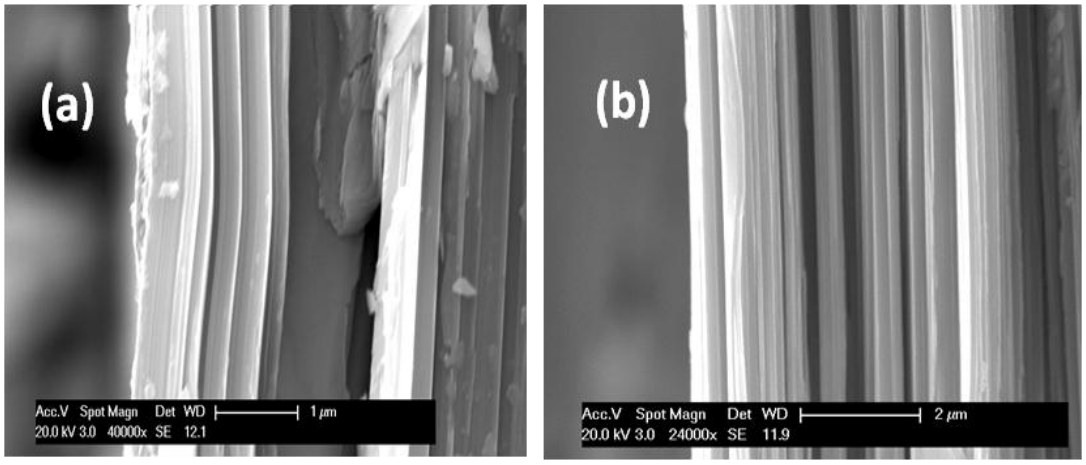

Figure 7.10: Cross-sectional SEM images of the stacked pseudo-superlattices (a) before and (b) after annealing at 250^0C for 5 sec.

7.5 Summary

In conclusions, we studied thermoelectric properties of "pseudo-superlattices" prepared by staking of the "graphene-like" mechanically exfoliated of single-crystal Bi_2Te_3 films. We showed that *ZT* in such structures can be substantially increased via reduction of the in-plane and cross-plane thermal conductivity with preserved electronic properties. This will open up a new strategy since Bi_2Te_3 and related alloys are shown to be topological insulators. This fabrication technique can further be extended to other thermoelectric materials of the bismuth telluride family, e.g. Bi_2Se_3, Sb_2Te_3, etc. Eventually, it may become possible to achieve the pure surface transport regime through the Dirac surface states, topologically protected against scattering, and achieve the theoretically predicted strong enhancement of *ZT* over a wide temperature range.

Most recently, it was suggested theoretically that thermoelectric performance in Bi_2Te_3 and Bi_2Se_3 topological insulators can be increased at low temperature resulting from the tunable hybridization-induced band gap [18]. TIs have an unusual electronic structure with a single Dirac cone. The surface states from top and bottom surfaces hybridize and result in enhanced *ZT* at low temperature regime. At temperatures below 150 K, are important for Peltier cooling, the *ZT* of the thin TI has been shown to be significantly enhanced. This enhancement is due to the optimized Fermi level at low temperature which increases the thermoelectric power. If we consider the thermal conductivity at low temperature: the thermal conductivity of bulk semiconductors scales as 1/*T*, i.e., it drops very fast with increasing temperature in the relatively high temperature range, owing to the crystal inharmonicity via phonon-phonon umklapp scattering [38]. In superlattices, the presence of interface scattering as well as dislocation scattering significantly modifies the temperature dependence of thermal conductivity. For both in-plane and cross-plane directions of Si/Ge and $Si_xGe_{1-x}/Si_yGe_{1-y}$ super lattices, an opposite trend of *K*-*T* has been observed [40-44]. With the above motivation, we studied the thermoelectric performance of stacked Bi_2Te_3 'pseudo-superlattices' at low temperature regime [45].

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Chapter 8

Thermal Interface Materials with Graphene Fillers

8.1 Introduction

With continuous device scaling and design complexity, high power density and escalating hot spot temperatures have become difficult to manage [1-2]. Thermal management has become a critical issue because of the rapid increase in power dissipation from silicon chips. This situation has posed a need for improved thermal interface materials (TIMs) which facilitate heat transfer across interface by reducing the contact resistance between the heat-generating chip and heat-sinking units [3]. The selection of a suitable TIM material to fill the interface between a chip and a heat spreader is critical to the performance and reliability of the semiconductor device [4]. The effective thermal resistance at the interface between two materials is a sum of the resistance due to the thermal conductivity of the TIM and contact resistance between the TIM and the two contacting surfaces. This is expressed as [5]

$$R_{effective} = \frac{BLT}{k_{TIM} A} + R_{c_1} + R_{c_2} \qquad [8.1]$$

Where BLT is the bond line thickness, k_{TIM} is the thermal conductivity of the interface material, A is the area, R_{c_1} and R_{c_2} are the contact resistances of the TIM at the

boundaries with the two surfaces. To improve the heat dissipation across an interface it is important to minimize the value of $R_{effective}$ which can be achieved employing a TIM with high thermal conductivity. Hence, high thermal conductivity of TIMs is needed for high performance [6-7]. It has been suggested analytically that an increase in TIM thermal conductivity to ~7 W/mK can translate into an improvement of package thermal performance by 0.1 ^{0}C/W [8].

Recently, there has been a transition from polymer based TIMs to the ones with metallic particles and spheres as fillers to cope up with the demand of increased thermal conductivity [9]. Current TIMs are based on polymer or greases filled with thermally conductive particles such as silver or silica, which require high volume fractions of filler (up to ~70%) to achieve the thermal conductivity of about 1-5 W/mK of the composite.. The thermal conductivity enhancement by loading of the metal particles is limited by their thermal contact with each other and with the surfaces across which the TIM is applied [10]. For this reason, much academic attention is focused on search of new materials with high thermal conductivity to serve as fillers. There has been a recent progress in nanocomposites with carbon nanotubes (CNT) as fillers with an intension of enhancement in thermal conductivity of TIMs owing to the high thermal conducting properties of CNTs [11]. Other carbon fillers include graphite nanoplatelets (GNPs), graphene oxide nanoparticles (GONs), and graphene flakes derived by chemical processes. Several groups have reported enhancement in thermal conductivity of up to 125% per 1 wt % of CNT loading depending upon the alignment of CNTs in the matrix, their aspect ratio, anisotropy and purity [12-16]. Technical barriers with using CNTs as

fillers include the poor thermal contact between free-end CNT tips to the substrate, alignment and purity of CNTs [15] and the cost of CNTs.

Since its discovery, graphene, sp^2 bonded single carbon sheet, has attracted much attention owing to its novel mechanical, electrical and thermal properties [16-19]. One of its potential applications includes its incorporation into polymer matrices [16, 20]. The interest has been renewed with advances in the production of exfoliated graphene sheets in bulk quantities that are necessary for applications to composites. Thermal conductivity enhancement in epoxy of up to 3000% has been reported with GNP (graphite nano-platelet) loading of ~25 vol% [21]. This outstanding enhancement can be attributed to true two-dimensional geometry of graphene, reduced GNP/epoxy interfacial thermal resistance, and of course, very high thermal conductivity of single as well as few layers of graphene [22]. Interfacial thermal resistance between GNP/polymer has been reported to be at least one order of magnitude lower than that between CNTs and polymer [23]. In addition, it has been experimentally reported that graphene platelets significantly enhance mechanical properties of epoxy nanocomposites as compared to CNT fillers [24].

In this chapter, we studied metallic thermal interface materials with graphene as filler material. A series of graphene-epoxy composite samples were prepared by varying percentage of graphene into the epoxy matrix. Thermal conductivity of these composites was measured by "hot disk" technique. The room temperature thermal conductivity increases by ~500% with a graphene loading of ~5 vol %. Thermal conductivity enhancement in graphene-epoxy is attributed to the outstanding thermal conductivity of graphene, its enhanced specific area and two-dimensional geometry resulting in strong

filler-matrix adhesion. The proposed *graphene-epoxy* composites may embark a new promising pathway for graphene as a filler material for enhanced thermal conductivity of thermal interface materials.

8.2 Sample Preparation and Characterization

In this letter we studied the experimental investigation of thermal conductivity in graphene/silver epoxy composites. In essence, we studied the thermal conductivity enhancement (if any) in TIMs with metallic fillers as well as graphene fillers simultaneously. For our study, we chose the commonly used and readily available silver epoxy, which is pre-processed epoxy with silver particles as filler materials. This epoxy has two parts: Part A which is epoxy and Part B is the hardener. Graphene platelets were prepared by isolation of graphene sheets via density gradient ultracentrifugation (DGU) [25]. This aqueous solution phase approach is enabled by using planar amphiphilic surfactant sodium cholate (SC) [26]. In DGU, aqueous solution of graphite flakes is centrifuged in a density gradient fashion giving control on graphene sheet thickness. We further treated this solution thermally to reduce surfactants concentration present in the graphene films, further improving flake to flake contact [25]. This method offers several advantages and utilizes inexpensive and readily available source of graphene materials and have been already available commercially [27]. Figure 8.1 (a) shows the TEM image (FEI-PHILIPS CM300) of the graphene flakes synthesized by the above method and deposited on a standard TEM copper grid for imaging, and Figure 8.1 (b) shows the

corresponding diffraction pattern of the graphene platelet shown in Figure 8.1 (a). The selected area electron diffraction pattern (SAED) reveals that the graphene flakes are crystalline after all the processing steps.

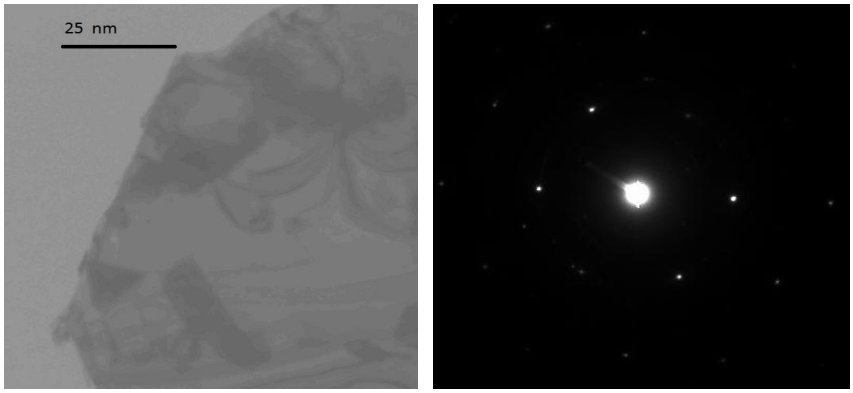

Figure 8.1: TEM image of a graphene flake deposited on a standard TEM copper grid, and (b) the measured electron diffraction pattern of the same flake.

For epoxy-graphene composite preparation, the desired amount of aqueous graphene solution was first measured and then was dispersed in the already weighed silver epoxy (part A) followed by high-shear mixing which was further followed by prolonged ultrasonication to ensure good dispersion. Part B of epoxy (hardener) was then added (equal weight to Part A) to the homogeneous mixture of graphene/epoxy Part A, followed by shear mixing. The homogeneous mixture of graphene solution and epoxy was then loaded into custom-made disk-shaped stainless steel mold and the nanocomposite was cured at room temperature for 24 hours. The mold had a diameter of

10 mm and a thickness of 1 mm. The dimensions of the mold were chosen to have suitable sample sizes which can be accommodated in the experimental technique we used to measure their thermal conductivity. The mold was cleaned using acetone and IPA to remove any surface contamination before transferring mixture into it. The residual solvent was removed by baking the mold (containing composite mixture) at 120 ^{0}C for ~10 minutes, which is typical curing temperature of this conductive epoxy (values provided by the supplier). The samples were further baked at 80 ^{0}C for 15 hours to remove remaining solvent and air bubbles from the silver epoxy/graphene composites (if any). Several epoxy/graphene specimens were prepared with graphene loading varying from 0.5 to 3 weight %. For comparison, silver epoxy composites filled with carbon black (Asbury Graphite Mills, Inc.) were also prepared using the same above-mentioned procedure. Figure 8.2 (a) shows the schematic of the stainless steel mold, and (b) silver spoxy/graphene molded disks.

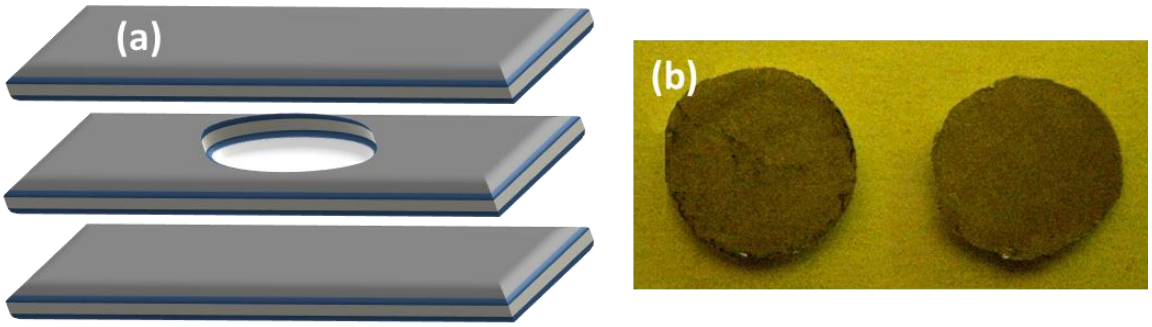

Figure 8.2: (a) schematic of stainless steel mold (b) optical image of silver epoxy/graphene composites investigated for TIM applications. Nano-Device Laboratoty, UCR.

Figure 8.3 shows the SEM image of graphene/silver epoxy composite disk. The grains seen in the SEM image are the silver particles. To verify the graphene content in the mixture, electron dispersive spectrum (EDS) was taken on different points. Figure 8.4 (a) and (b) shows the EDS spectrum at two different points indicated as 1 and 2 in Figure 8.5, indicating graphene content at places in between the silver grains.

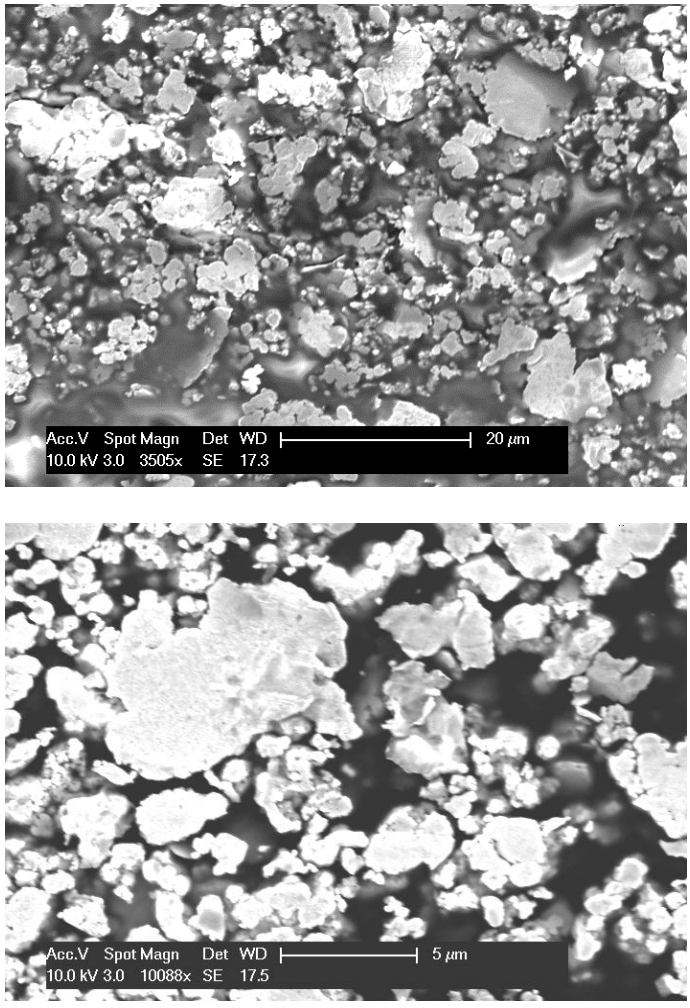

Figure 8.3: SEM scan of graphene/silver epoxy composite sample.

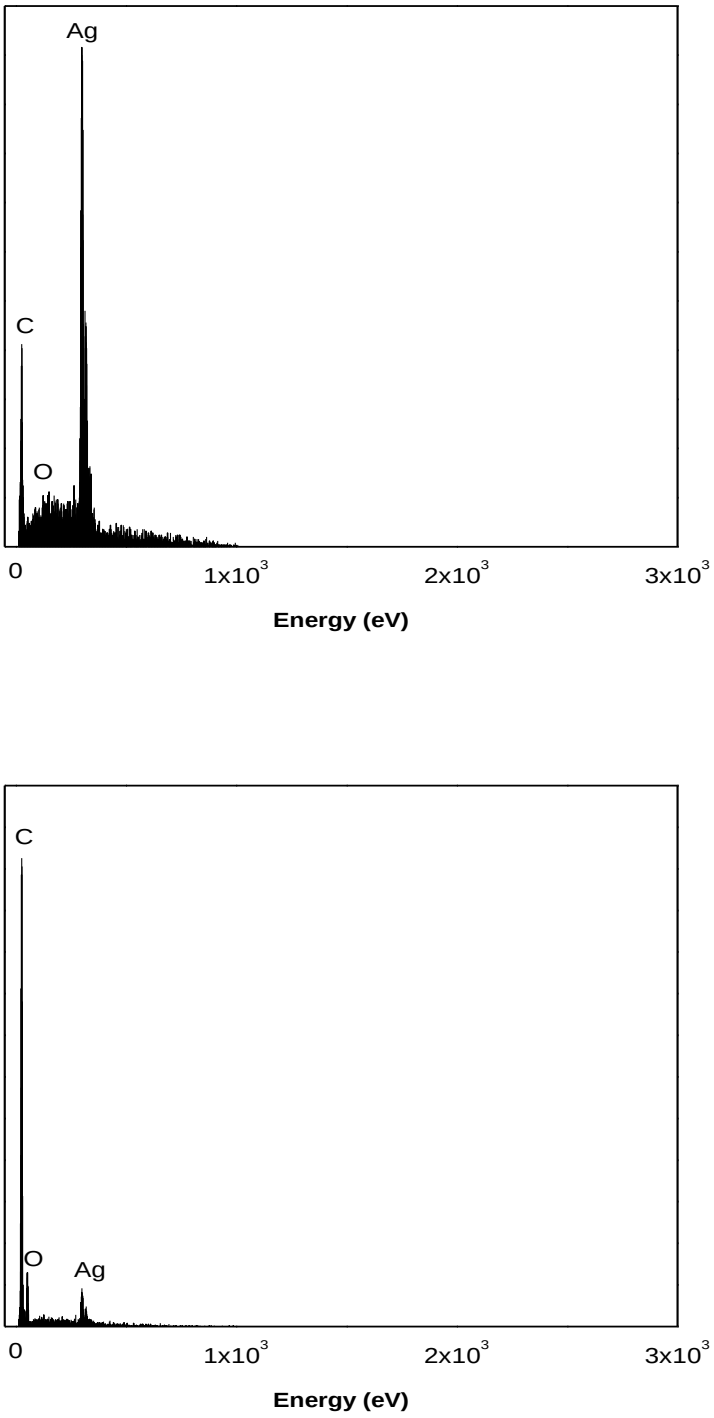

Figure 8.4: EDS spectrum of graphene/silver epoxy composites at two different points showing the presence of carbon (graphene) on top and in-between some of the silver grains.

8.3 Thermal Conductivity of Graphene/Epoxy Composites

Thermal conductivity of the base silver epoxy and silver epoxy/graphene composites with different mass/volume fraction of graphene was measured using transient plane source hot-disk technique (Hot Disk TPS2500 S, Hot Disk AB Company, Sweden) [28]. The hot disk technique have been used as a thermal conductivity measurement tool for expanded graphite (EG)/paraffin composite phase change materials (PCMs) [29] as well as for thermal greases by industry (Intel Corporation) [30]. The working principle of our hot disk instrument has been explained earlier in Chapter 3. The thermal conductivity was measured by sandwiching an electrically insulated flat disk-shaped nickel sensor with radius 2.001 mm in between two identical samples of same composition epoxy/graphene composite. The sensor behaves as the heat source and the temperature monitor simultaneously. The surfaces of the specimen were flattened and cleaned to reduce contact resistance between the sensor-sample surfaces. Interfacial thermal resistance between nickel-kapton (insulating layer) was taken care by the software itself [28, 30]; and between sample-sensor surface was separated by using data points generated after short time t for thermal diffusivity calculations [31]; t is the time after which the average temperature rise in the sample due to applied electric pulse becomes constant.

Ten specimens of each composite with different graphene weight fraction were prepared and measured using TPS system to guarantee the repeatability of the data. Figure 8.5 shows the measured thermal conductivity of pristine silver epoxy, graphene/epoxy composites with different graphene percentage, and carbon black/epoxy

composites. The error bars represent the data scattering based on measurements of different number of samples.

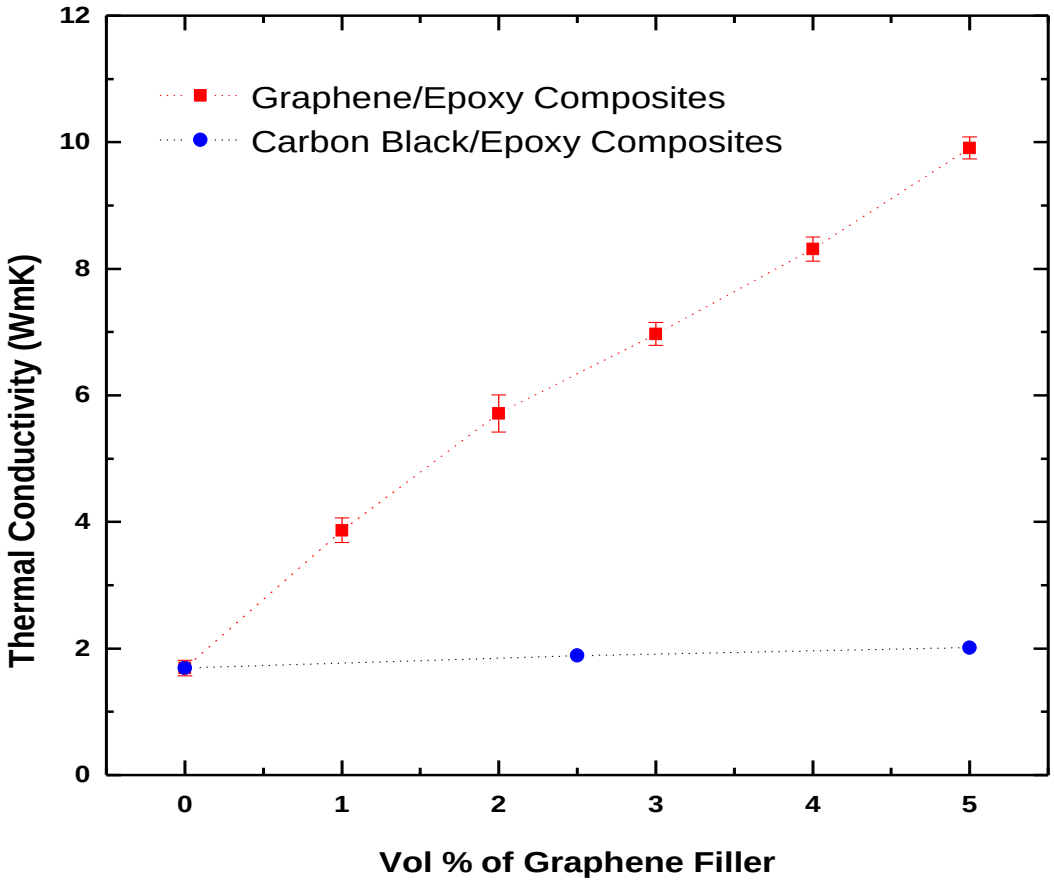

Figure 8.5: Thermal conductivity of pristine silver epoxy, silver epoxy/graphene composites and silver epoxy/carbon black composites as a function of vol % of graphene filler.

The thermal conductivity of the composites increases greatly with increase in the mass/volume fraction of graphene. The thermal conductivity of pristine silver epoxy was measured to be ~1.67 W/mK (value provided by the supplier ~1.6 W/mK). Thermal conductivity value of the epoxy/graphene composite with 5 vol % of graphene reached to ~9.9 W/mK, more than 6-folds higher than that of pristine silver epoxy, which is equivalent to 500% increase in thermal conductivity. Only solid parts were used for the calculations of weight fraction which includes graphene, epoxy (resin+hardener) and surfactant (sodium cholate, used to wrap the graphene flakes) iodixanol (molecule used in the purification process) [22]. The weight fraction was then converted to volume fraction using volume fraction equation for fibrous composites given by [27]

$$V_{GF} = \frac{W_{GF}}{[\{W_{GF} + (\rho_{GF} / \rho_{epoxy})(1 - W_{GF})\}]} \qquad [8.2]$$

where, V_{GF} and W_{GF} are the volume and weight fraction of graphene flakes, ρ_{GF} and ρ_{epoxy} are the densities of graphene and silver epoxy respectively. Density of silver epoxy (*resin + hardener*) was determined to be ~4 g/cc. Density of graphene can be estimated to be ~2.2 g/cc. The volume of the graphene unit cell is equal to

$$V_0 = 3\sqrt{3}a^2 h \qquad [8.3]$$

where a = 0.142 nm and thickness of grapheme layer h = 0.35 nm. The unit cell consist of 2 carbon atoms, so mass of the unit cell $m = 2M_{carbon}$. Therefore, graphene density is given by

$$\rho = m/V_0 = 2M_{carbon}/V_0 \approx 2.2\, g/cc \qquad [8.4]$$

Using above values, the weight fraction of 0.53 % translates into ~1 vol %, etc.

Temperature dependent study on thermal conductivity was also done on these samples. Figure 8.6 shows the Thermal conductivity as a function of temperature for epoxy/graphene composites with 1, 3, and 5 vol % of graphene. The thermal conductivity of these samples slightly increases with temperature over the investigated temperature range, which was chosen with-in the operating temperature of silver epoxy. This *K*-*T* dependence is consistent with the general trend for highly disordered dielectric materials [28]. Scattering of phonons at the surfaces of graphene flakes and silver grains may also increase the suppression of heat conduction.

Electrical properties were also studied on these composites using 4-probe resistivity measurements (Signatone and HP4142). The electrical resistivity of pristine silver epoxy was measured to be ~10^{-4}ohm-m. The electrical resistivity does not change much with addition of graphene. This may be attributed to the fact that the epoxy itself is highly conductive and so, graphene flakes do not enhance it further. But on the other hand it is interesting that even by increasing the number of interfaces by incorporation of graphene, the electrical properties are not affected.

For comparison, in Table 8.1, we list representative data for thermal conductivity enhancement factor in the composite carbon materials, the enhancement factor is defined as [32]

$$\eta = (K_e - K_b)/K_b \qquad [8.5]$$

where K_e is thermal conductivity of the carbon composite material and K_b is the thermal conductivity of the base material. We observed 500% enhancement for graphene/silver

epoxy composites and 1000% enhancement for graphene/epoxy composites at 5.0 vol% fraction of graphene. The thermal conductivity of 9.9 W/mK achieved for graphene/silver epoxy composites at 5 vol% is exceptional.

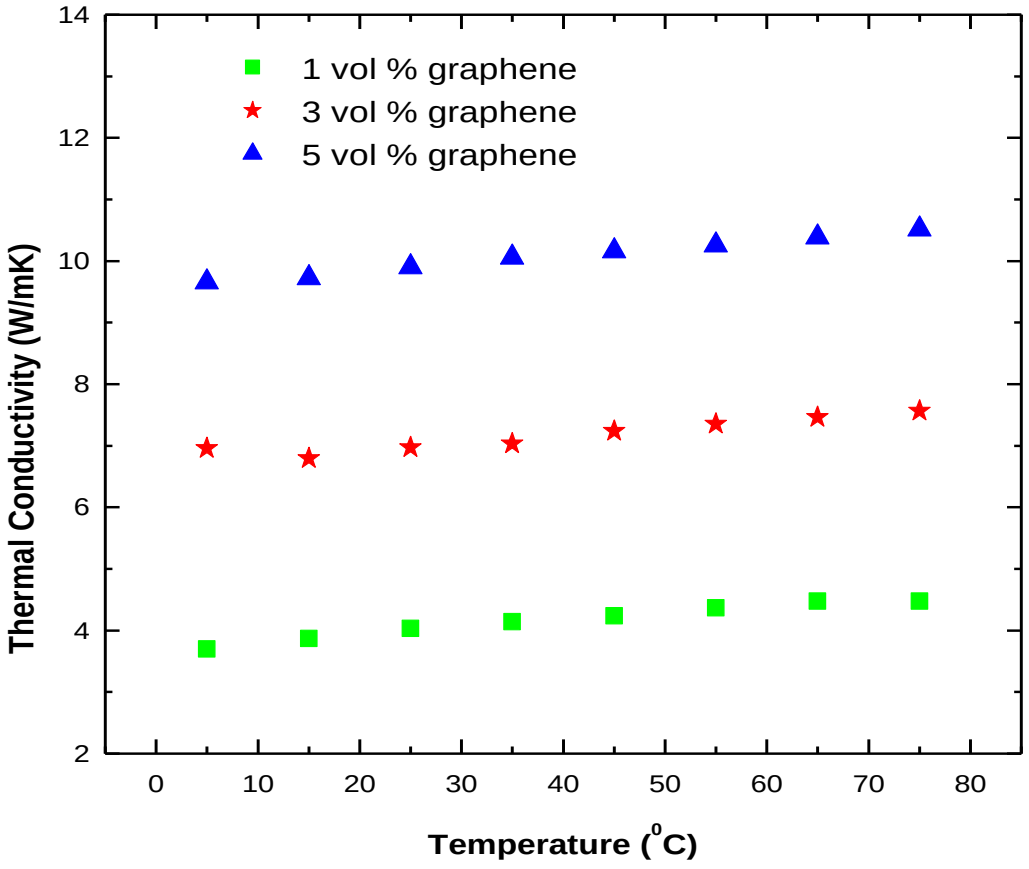

Figure 8.6: Thermal conductivity as a function of temperature for epoxy/graphene composite with 1, 3, and 5 vol % of graphene.

Table 8.1 Thermal Conductivity Enhancement in nanocarbon composites

Filler	*Enhancement*	*Fraction*	*Base Material*	*Reference*
MWNT	150%	1.0 vol%	oil	Choi *et al*. [33]
SWNT	125%	1.0 wt%	epoxy	Biercuk *et al*. [13]
SWNT	200%	5.0 wt%	epoxy	A. Yu *et al*. [15]
CNT	65%	3.8 wt%	silicone Elastomer	C. H. Liu *et al*. [12]
GNP	3000%	25.0 vol%	epoxy	A. Yu *et al.* [21]
GON	30% - 80%	5.0 vol%	glycol; paraffin	W. Yu *et al*. [35]
Graphene Oxide	400%	5.0 wt%	epoxy resin	Wang *et al*. [36]
Graphene	500%	5.0 vol%	silver epoxy	Goyal *et al*. [34]
Graphene	1000%	5.0 vol%	epoxy	Shahil *et al*. [32]

Despite variations in the thermal conductivity enhancement explained by different base materials and composite preparation methods, the general conclusion is that graphene, CNTs and nanoscale graphite particles are effective as filler materials in terms of the resulting K_e values. Our data indicates that graphene flakes can outperform CNTs and other carbon materials owing to their geometry and better coupling to base materials, which leads to stronger enhancement at a given loading fraction, and lower cost. Thermal boundary resistance reduction is the key to better graphene/TIM composite performance. It has been shown that thermal boundary resistance between graphene and substrate is

independent on the substrate; and is rather low on the order of ~10^{-8} m^2K/W [37-43]. The observed enhancement factors with carbon materials are not achievable with conventional fillers.

8.4 Simulation of Transient Heat Transport in Flip-Chip Package with Graphene/Silver Epoxy Composites

To obtain estimates for the hot spot temperature reduction as a result of higher thermal conductivity of TIM (graphene/epoxy composites) we simulated *T* profiles in a flip-chip package. The heat diffusion equation for given package structure was solved numerically by the finite-element method using COMSOL software. The heat conduction was modeled by solving numerically Fourier's law. The devices were modeled as heat sources with the power density and geometry chosen in such a way so that the resulting temperature rise is close to the typical values in state-of-the-art chips. In our model we approximate five active devices as heat generating element. Each source has the width and thickness of 50 nm and 25 nm, respectively (see Figure 8.7). The linear power density of each active channel was set to 0.3 W/mm. The heat sources were separated from each other by 10 μm. The heat spreader attached to the device structure with TIM1 and the heat sink attached with TIM2 is considered to be bulk copper with a thermal conductivity of 400 W/mK.

Throughout simulation, we have observed the effect of graphene/silver epoxy on temperature rise within the chip. The conventional metallic TIM (silver epoxy) with thermal conductivity of 1.6 W/mK was then replaced with the graphene/silver epoxy

composites. The actual thermal conductivity (measured in this work) of ~10.52 W/mK (at 75 ^{0}C, which is the operating temperature of state-of-the-art electronic chips) was taken into account. Figure 8.8 (a) and (b) are the temperature profiles across the modeled circuit with five active transistors with metallic TIM and graphene/silver epoxy composite, respsctively. The difference in the maximum device-channel temperature rise, ΔT_m, between silver epoxy TIMs (TIM1 and TIM2) and graphene/silver epoxy TIMs was found to be ~80 ^{0}C.

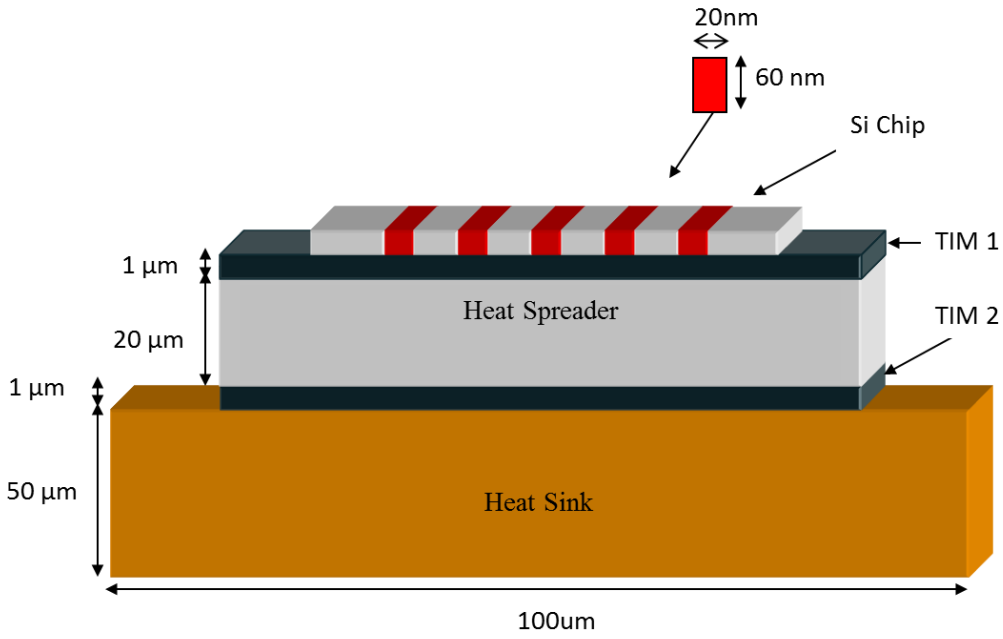

Figure 8.7: Schematic of a flip-chip package with TIM1 and TIM2 attaching Si chip to heat spreader and then to heat sink. The thicknesses are not to scale.

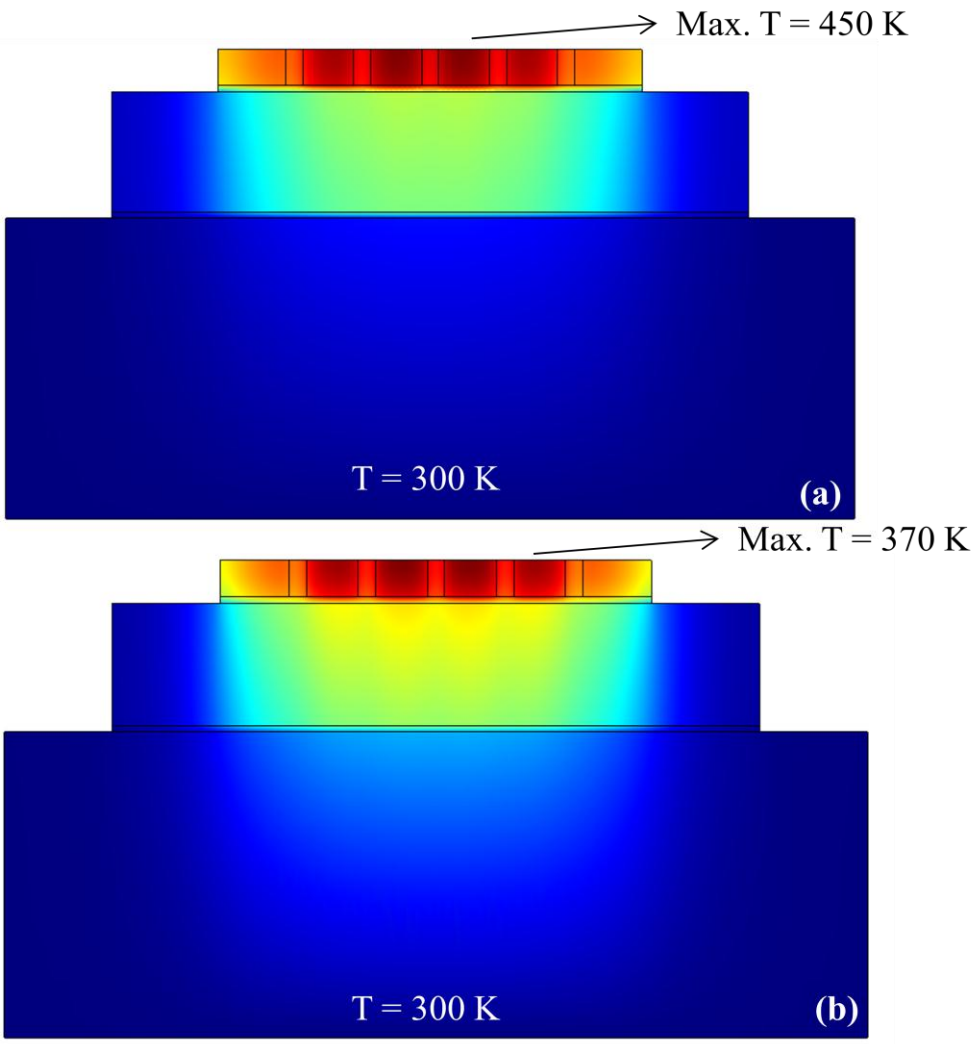

Figure 8.8: Temperature distribution across the modeled circuit with five active transistors on Si chip with (a) silver epoxy – metallic TIMs and (b) graphene/silver epoxy composite TIMs.

The simulation results show that replacement of conventional silver epoxy by graphene/epoxy composites will translate into an improvement of package thermal performance, the chip will run at cooler temperatures with reduced hot spot temperatures, thereby increasing lifetime as well as reliability of the chip/device. It is clear from the

Figure 8.9 that graphene/epoxy composites provide less resistance to heat flow at the interface owing to their higher thermal conductivity (~557% enhancement, at 75 ^{0}C) and are far better that conventional TIMs in terms of thermal management.

8.5 Summary

In this letter, we used the low cost produced liquid solution of graphene and few-layer graphene flakes to produced graphene/epoxy TIMs with graphene as the filler material. We experimentally demonstrated that graphene flakes can substantially increase the thermal conductivity of the composite materials even at small volume loading fractions. The thermal conductivity enhancement exceeded a factor of five at 5% of the volume loading fraction. This enhancement is far higher than that of CNT/epoxy composites owing to their geometry and better coupling to base materials, which leads to stronger enhancement at a given loading fraction, and lower cost.

At the same time, the future applications of graphene in TIMs would eventually depend on several other factors including the viscosity of the composite, filler – matrix coupling, coefficient of thermal expansion (CTE), thermal interface resistance and cost of production [44]. An important characteristic for TIM applications of graphene is its high temperature stability, which was verified up to 2600 K [45]. The use of liquid-phase exfoliated graphene [46] in advanced TIMs can become the first industry application, which would require large quantities of this material [47].

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Chapter 9

Conclusions

9.1 Summary of Dissertation

This dissertation explored thermal transport in several advanced engineered materials such as thin films and superlattices designed for possible applications in electronics. It provides insights into the material parameters, which can be used to tailor the thermal properties. The specific material systems, which were studied in this dissertation, are briefly described below.

The chemical vapor deposition grown ultrananocrystalline diamond and microcrystalline diamond films on Si are potential candidates for thermal management. We investigated their thermal resistance in comparison with the conventional Si wafers. The thermal conductivity of these samples was measured in a wide temperature range from 25 ^{0}C to 250 ^{0}C using TPS technique. It was found that the Si-synthetic diamond composite substrates reveal different temperature dependence of the thermal conductivity than the conventional Si wafers. I demonstrated that the composite substrates can outperform Si in terms of thermal conduction at elevated temperatures characteristic for the operation of the state-of-the-art electronic circuits. The benefit of the composite substrates increases with the growing power density and operation temperature of the chips. The simulation results show that incorporation of MCD/Si and UNCD/Si

composite substrates lead to substantial reduction in temperature of the hot spots and corresponding increase in the carrier mobility. The obtained experimental results shed light on dependence of the thermal conductivity of Si/synthetic diamond composite substrates on the polycrystalline diamond grain size, film thickness and thermal boundary resistance at the Si/diamond interface.

The high-power electronic devices on the basis of GaN often suffer from the problem of overheating. In collaboration with the Argonne National Laboratory (ANL), we examined a possible new approach for their thermal management. The samples produced at ANL were integrated high-quality nanocrystalline (NCD) diamond film grown directly on GaN substrate at low substrate temperatures (~450 ^{o}C). The detail characterization of NCD/GaN structures by Raman spectroscopy revealed no changes in the GaN structure after the diamond deposition process. In a set of measurements in the Nano-Device Laboratory, I experimentally demonstrated that the thermal conductivity of NCD/GaN substrates is better than that of GaN and Si at elevated temperatures, which are characteristic for operation of state-of-the-art high-power electronic devices. I also proposed possible strategy for improving the thermal management of GaN electronics. The maximum achievable power density of GaN based devices can be increased further by optimizing the chip-size, the grain size in NCD layers and film thickness.

In this dissertation research we also investigated the thermal conductivity of free standing polycrystalline graphene (PCG) and graphene oxide (GOx) films, which were synthesized in the University of Manchester, U.K. The thermal measurements on these films were carried out using the Raman optothermal technique, which was originally

developed for thermal conductivity measurements of the single-layer graphene (SLG). The finite-element simulations with the COMSOL software tools were utilized for the experimental data extraction. The thermal conductivity dependence on the grain size and density of the flakes, phonon scattering on polycrystalline grain boundaries and structural defects was studied in details. The thermal conductivity of the PCG/GO films was found to be far less than that of SLG. At the same time, it increases with the increasing grain size and the density of the flakes. As the grain size grows, the thermal conductivity can become larger than that of the thin copper films.

Continuous search for materials with the high thermoelectric figure of merit, ZT, calls for exploring thermal properties of newly discovered materials with potential for thermoelectric applications. It was theoretically suggested that thin films of topological insulators can have strongly enhanced ZT in a wide temperature range. Motivated by these theoretical studies, carried out at University of California – Riverside and University of California – Berkeley, I investigated thermoelectric properties of "pseudo-superlattices" prepared by staking of the "graphene-like" mechanically exfoliated films of single-crystal Bi_2Te_3. Using the exfoliation technique developed for Bi_2Te_3 family of materials in the Nano-Device Laboratory, I designed and fabricated the stacked 'pseudo-superlattice' structures suitable for thermal and electrical studies. I have experimentally showed that *ZT* in such structures can be increased by up to 250% via reduction of the in-plane and cross-plane thermal conductivity without degradation of the electronic properties. I have also studied the annealing effects on the thermal conductivity of stacked "pseudo-suparlattices" made of Bi_2Te_3, Bi_2Se_3, Sb_2Te_3, and other materials of

this family. It is expected that eventually, it becomes possible to achieve the pure surface transport regime through the Dirac surface states, topologically protected against scattering, and achieve the theoretically predicted strong enhancement of *ZT* over a wide temperature range.

The last section of this dissertation research deals with the thermal interface materials (TIMs). The improvements in TIMs can have a profound effect on heat removal from electronic circuits, optoelectronic and photonic devices. I have produced liquid solution of graphene and few-layer graphene flakes to fabricate graphene/epoxy TIMs with the carbon materials as the fillers. I experimentally demonstrated that graphene flakes can substantially increase the thermal conductivity of the composite materials even at small volume loading fractions. The thermal conductivity enhancement exceeded a factor of five at 5% of the volume loading fraction. This enhancement is far higher than that of CNT/epoxy composites and was attributed to the geometry of graphene flakes and its better coupling to base materials. An important characteristic for TIM applications of graphene is its high temperature stability, which was verified up to 2600 K. The use of liquid-phase exfoliated graphene in advanced TIMs can become the first major industry application.

9.2 Competitive Awards Won During the Dissertation Research

1. Recipient of UC-Riverside *Dean's Dissertation Year Fellowship Award* (2011)
2. Recipient of *Dean's Distinguished PhD Fellowship Award*, Bourns College of Engineering, University of California-Riverside (2008-2010)
3. Recipient of *MRS Award* for Functional Two-Dimensional Layered Material Research, Symposium Y, MRS Spring Meeting, San Francisco, CA, April 26-29, 2011.
4. Recipient of *MRS Poster Award* (co-author), MRS Spring Meeting, San Francisco, CA, April 2011. Poster title: **"**Fabrication and Characterization of Electrically Gated Graphene-on-diamond Devices."
5. Recipient of *Young Scientist Award* (co-author), 38th conference on the Physics & Chemistry of Surfaces & Interfaces (PCSI-38), San Diego, CA, January 16-20, 2011.
6. Demonstrated exceptional performance in graduate school by completing M.S. and Ph.D. degrees in a total time period of three and half years.

9.3 Peer-Reviewed Journals Resulted from the Dissertation Research

1. Goyal, V., Sumant, A.V., Teweldebrhan, D. and Balandin, A.A., "Direct Integration of Nanocrystalline Diamond with GaN Substrate for Improved Thermal Performance," (Under review: submitted to *Nano Lett.*).

2. Goyal, V., Teweldebrhan, D., and Balandin, A.A., "Pseudo-superlattices of Bi_2Te_3 Topological Insulator Films with Enhanced Thermoelectric Performance," *Proc. of MRS 2011* (Accepted, Manuscript ID: MRSS11-1344-Y12-08).

3. Yu, J., Liu, G., Goyal, V., Sumant, A.V. and Balandin, A.A., "Top-gate Graphene-on-UNCD Transistors with anced Performance," *Proc. of MRS 2011* (Accepted, Manuscript ID MRSS11-1344-Y03-09).

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