Thermal Characterization and Simulation of a fcBGA-H device

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Abstract

In this paper, the thermal performance data of theta jc (Rth-JC) and theta ja (Rth-JA) of a flip chip ball grid array device with heat spreader, fcBGA-H, is measured. For Rth-JC, various boundary conditions for the thermal resistance modeling are considered and discussed. A transient measurement method is used to obtain the temperature responses of the diodes, as a function of time. The structure functions of the diodes are measured, and based on the structure functions, the thermal resistances are calculated. With the structure functions, the impact of package configurations are better viewed and demonstrated, and a novice measurement technique is also proposed here to measure the thermal resistance of junction to die, Rth-JD. With this experimental setup, there is no need to use the thermal couples. The traditional drilling hole for thermal couple and thermal couple itself will change the package configuration and heat dissipation path, and, therefore, impact the accuracy of the measurements.

Keywords: TIM, thermal resistance, junction temperature, flip chip, structure function

(1) Introduction

Flip-chip packages are commonly used for various applications such as desktop computers, servers, telecommunications, gaming, etc. Due to tremendous demand of die functionality, the power levels and more importantly the die heat-flux densities are drastically increasing, thus customers are constantly pushing packaging industries to lower thermal impedance of thermal interface material (TIM) for very high power flip chip packages.

TIMs are thermally conductive materials used to increase the thermal contact conductance across jointed solid surfaces, such as between CPUs and heat spreaders. If there is tiny air gap, which is a very poor conductor, filled at the interfaces with contacted solid surfaces, the efficiency of heat dissipation will be drastically deteriorated. For this regard, the thermal characterization of the TIM has been a crucial work to meet the thermal specification for the reliability, especially the parameters of the highest temperature on the die (Tj), the temperature on the top of the heat spreader (Tc), and the thermal resistances between these two spots or locations [1]. The traditional way of the measuring the case temperature (Tc) is to use a thermal couple at the center of the heat spreader. The major problem with this classical measurement standard is that it requires the case temperature to be at center but in real applications the location of the hottest point may be unknown especially when the die is heated with non-uniform power.

In this paper, the goals are to (1) measure the thermal performance of TIM on an assembled flip chip ball grid array device manufactured at STATS ChipPAC using the transient measurement techniques [2] without the need of thermal couple (2) measure the thermal performances of the packages with cooling fans (3) correlate the simulation data with experimental data (4) identify and propose the best reasonable simulation and experimental approaches (5) suggest better testing method for thermal community, and the details are explained in the followings.

(2) Configuration of the Package

To evaluate the thermal performance of TIM, a flip chip test vehicle is built internally at STATS ChipPAC and the configuration is shown as in the Figure 1 and 2 below. The test package includes following components, from

top to bottom, a 25x25x1mm copper heat spreader, a TIM layer, a layer of underfill and solder bumps, a 12 layers substrate with total thickness 1.65mm, an array of solder balls, and a PCB. On the side, the epoxy material is used to bond the copper lid with the substrate.

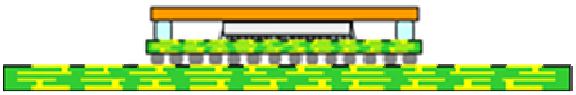

Figure 1. The demonstrated side view of the test vehicle

Figure 2. The top view of the real test vehicle

The full coverage of TIM on the die is carefully processed and the thickness of the TIM is monitored and controlled to be around 38um with the tolerance smaller than 2um, as shown in the Figure 3 and 4 below. The thickness control is through the mechanical press applied on top of the heat spreader right after the TIM dispensing, and during the curing process.

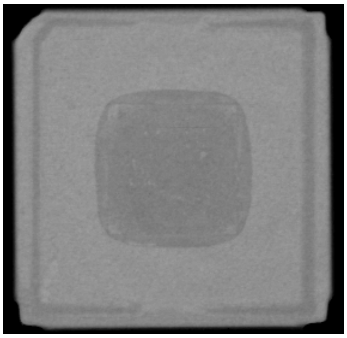

Figure 3. TIM Coverage

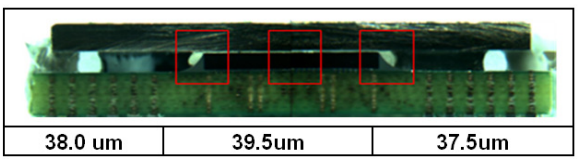

Figure 4. TIM thickness measurements

(3) Thermal Simulation of Thermal Resistance (Rth)

The thermal simulation tools have been very popular in the prediction of the thermal performance of the IC packages. The early stage of thermal modeling could help predict the thermal reliability of the IC packages and provide important factors for system-level thermal evaluation and optimization. For lots of situations, instead of real thermal testing, the modeling is heavily utilized to avoid the time-consuming and costly experiments. In this paper, the thermal resistance of junction-to-case, Rth-JC, which is one of the most important thermal parameters, especially for the flip chip devices, is numerically studied [3,4,5]. However, several cases of Rth are modeled and compared in detailed below.

Fixed Rth-JC vs. Floating Rth-JC

The fixed case Rth-JC here refers to that the top of the lid is assumed to be fixed at a constant temperature as shown in Figure 5. For this configuration, the heat dissipation toward the lid top is in vertical or in out-of-plane direction, and it has less in-plane heat spreading inside the lid, while the floating case Rth-JC allows the temperatures on the top of the lid to vary depending on the cold-plate conditions. To study the impacts of the configurations, the location of traditional case temperature, T_c, is shown as in the equation below.

$$\text{Rth-JC} = (T_j - T_c) / \text{Power}$$

where the Tc refers to the temperature at the top center of the heat spreader.

For the floating Rth-JC, two configurations are considered here. The first one is a cold plate with a cooling fluid inside, and the second one is that the cold plate being replace by a similar size of copper block and assuming that the top of the block is kept at a constant temperature. The boundary conditions of the three configurations are shown in the Figure 5 below. The CFD and heat conduction simulation are conducted to calculate the Rth-JC of all the configurations.

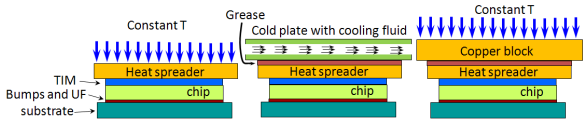

Figure 5. Boundary conditions for Rth-JC modeling, fixed case, cold plate, and copper block.

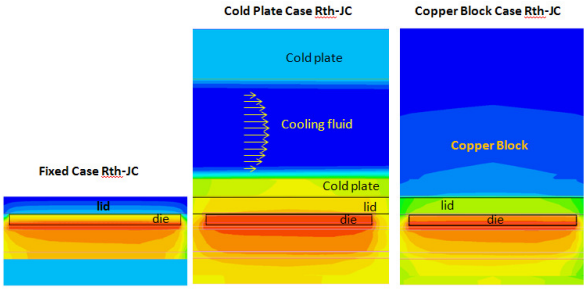

Figure 6. Temperature distributions near the die and lid

Figure 6 illustrates the simulation result of the temperature distributions from the three different configurations, and the Rth-JC data is calculated and listed on Table 1. The Rth-JC from the fixed case is about 15-20% higher than the ones from cold plate and copper block. The cold plate configuration is the most comprehensive consideration of the real situation, however, several serial of modeling cases indicate that the copper block case is a quick, simple, and reasonable approximation to obtain more real-world Rth-JC data.

Configuration	Top Lid Surface Temperature	junction T	Case T	Rth-JC	Rth-JP
Fixed Case	constant (20C)	20.351	20	0.117	0.117
Cold plate	vary by locations	21.712	21.422	0.097	0.128
Copper block	vary by locations	20.839	20.537	0.101	0.126

Table 1. The thermal resistance data

Point Case Rth-JC vs. Plane Case Rth-JP

The data of the Rth-JC provides a very good way to predict the junction temperature of the package. The case temperature is referring to the point at top center of the lid surface. However, as just mentioned earlier, the Rth-JC is affected by the non-vertical heat dissipation direction inside the lid, and another ambiguity is that the highest top lid surface temperature may not be at the center, especially when the heating of die is non-uniform. For this regard, a new thermal parameter, Rth-JP, thermal resistance from junction to the plane, is defined here.

$$\text{Rth-JP} = (T_j - T_P)/\text{Power}$$

where the "plane" here refers to an area, the same size as the chip, but located exactly at the top lid surface, and Tp is the averaged temperature of the area. The usage of the Tp, although not a perfect one to fully describe the heat spreading resistance, shall be a better parameter to represent the thermal resistance between the junction and the top lid surface. In this study, uniformly distributed 25 data points, as shown in Figure 7, at the plane are used to calculate the average temperature, and the data of Rth-JP is again listed on the Table 1. The data shows that, for both cold plate and copper block cases, the Rth-JP is higher than the Rth-JC. The Rth-JP here is a simulation parameter which is not supposed to be measured by experiment because of too many points involved.

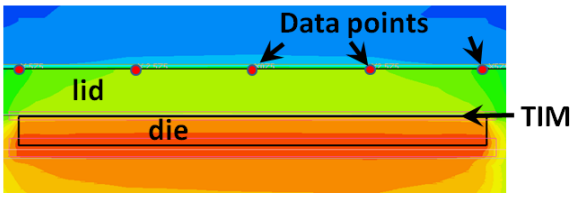

Figure 7. Data points for Rth-JP calculation

Determination of the Effective Thermal Conductivity of TIM layer

The main obstacle of getting the accurate thermal resistance of the TIM on the package, when compared with the real world thermal data, is the true "effective" thermal conductivity of the TIM layer. The total effective thermal conductivity of the assembled TIM layer on the package, most of the time, is different from those given bulk thermal conductivity data from the manufacturers. The reasons are due to the voids formation, density variation, non-uniformity of the thickness, kinetic behavior during the thermal loading, thermal resistances at contact surfaces, and the processing factors on the assembled devices.

To determine the true effective thermal conductivity of the TIM layer, the common procedure is to manufacture several test samples with different TIM thicknesses, and from the measurements of the temperatures inside the test samples, the effective thermal conductivities of TIM layers can be plotted as a function of the thicknesses. The disadvantages of the approach are that the thermal conductivity could be very nonlinearly dependent of the thickness and lots of samples may be needed, due to the fluctuation of the test data, to

determine the thickness-conductivity relationship. On this paper, the TIM thickness over 50 um is not permitted because of the thermal budget of the device. Therefore, all the thicknesses of the packages are controlled near 38um, without other different experimental TIM thicknesses to estimate the effective thermal conductivity of the TIM layer as a function of the thickness. The determination of the effective conductivity of TIM must rely on the single available thickness in the experiment. To do so, the procedure of the calculation is shown in Figure 8. Initially, a thermal conductivity of TIM layer is assumed to simulate the Rth-JP of the device then compared with the experimental Rth-JC. When the difference (Δ) is larger than the spec (S), another different of the thermal conductivity of TIM layer is repeated. The iteration keeps going until the tolerance is met. In this study, we have found that the effective thermal conductivity is different from the given data provided by the TIM vendors.

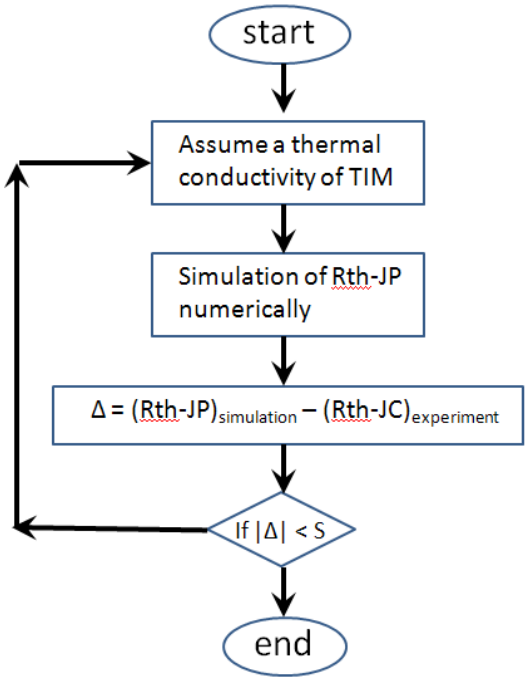

Figure 8. The simulation procedure to determine the effective thermal conductivity of TIM

(4) Measurement Methodology

In this paper, the transient measurement technique is used, and the measurement system is T3ster from Mentor Graphics. The system uses the response of the transient temperature of the package to determine the thermal characteristics of the package[6]. In theory, two thermal measurement approaches can be used. The first one is that the package is supplied by a small constant current and is kept at a low steady state temperature without heating the package. Then supply a larger constant current to heat the package and the temperature increment of the package is monitored as a function of time. The second approach is that the package is held steadily heated with two constant currents. Then shuts off the larger current, and the response of decreasing temperature is recorded. Both the increasing and decreasing responses of the temperatures depends on the structure of the package, such as dimension, configuration, heat capacity, thermal conductivity, and so on. With the powerful numerical analysis of the system, the thermal resistances and the heat capacities of the components on the package can be determined and identified. Theoretically, both the heating and cooling approaches work well for the measurement, but cooling approach is used in this paper for its fast transient, better stability, and lower noises.

To study the thermal resistance in between the junction and the lid's top surface, one good and one bad grease materials are used to interface with the cold plate as shown in the previous Figure 5. The use of bad grease material, which has very low thermal conductivity, guarantees a good contact at the interface without the issues of big air gap at the interface due to either surface non-uniformity or warpage. Also, it provides a smoother curve of the response data without the risks of the discontinuity of the measured data. The use of the bad grease material is a minor tweak from the JEDEC51-14, for which no grease is used for one case. Figure 9 illustrates a typical figure of the structure function, and Figure 10 illustrates the figure of the separation of the structure from the JEDEC 51-14 standard, where the blue color curve is with grease material while the red curve is without grease material. To clearly determine the point of separation between the two curves, the differences of the two curves may be calculated numerically to obtain the difference of structure functions.

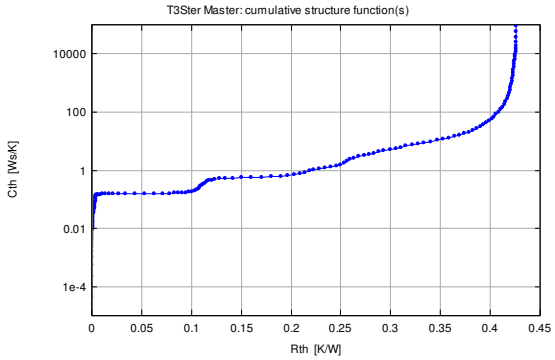

Figure 9. The structure function

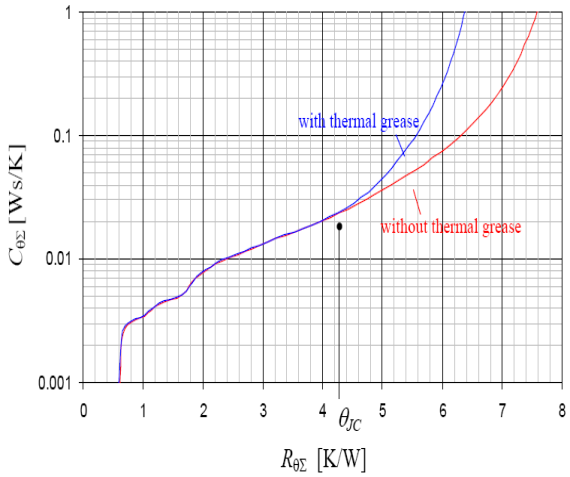

Figure 10. The structure functions with and without greases from JEDEC 51-14 standard.

Thermal test die

Thermal test dies have been widely used in the package design qualification. Figure 11 shows the thermal test die, which is 10x10mm, being used in this experiment. The die has 4X4 = 16 cells, and each cell can be used individually, or some cells can be connected together depending on the needs of the test conditions, such as, uniform heating or non-uniform heating. There are 10 diodes sensors populated on the die to measure the temperatures either at the center, at the sides, or at the corners. In this test, all the 4x4 cells are used to generate a uniform heating of the die. Figure 12 shows that the resistors on each row are connected together. To power the entire die all together at the same time, all the row resistors have to be coupled together, and either a serial or parallel resistors can be used, as shown in Figure 12. However, the serial resistors guarantee a constant current flowing through all the resistors, while parallel resistors may cause the unbalance of the current magnitude between rows of resistors, especially when the length and width of the traces are different. Another concern of the parallel resistors is that, when the heating of the die is non-uniform, the center of die tends to be hotter than the peripheral of the die, and the high temperature may cause the local electrical resistance to get higher, and further deteriorate the unbalance. To avoid the potential risk of unbalanced of the electrical current, the connection of serial resistors is used here. For the experiment on this paper, an electrical current of 325mA is applied to the resistors and the total power is 23 Watts.

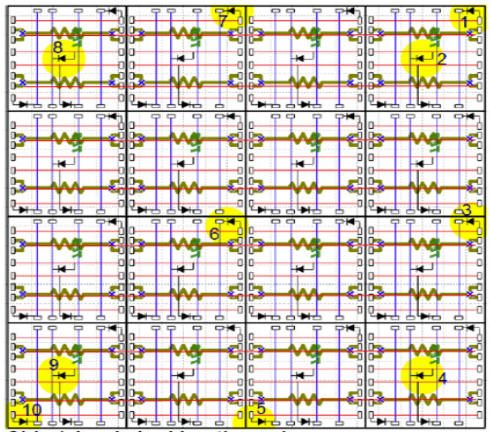

Figure 11. Test thermal die

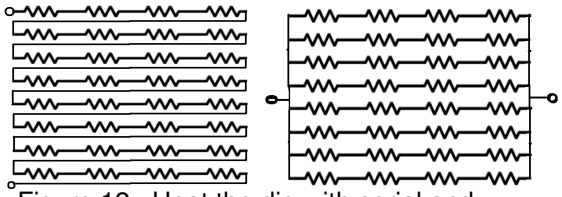

Figure 12. Heat the die with serial and parallel resistors

Calibration of the Diodes

As shown in the Figure 11 again, there are 10 diodes populated on the silicon die. The diodes are used for the measurements of the temperatures at various locations. As a small electrical current flow through the diode, the voltage drop across the two ends of the diode is linearly dependent on the temperature. Therefore, before the heating of the package, each diode is calibrated to get its voltage responses as a function of the temperatures, or thermal sensitivity data, and Figure 13 illustrates one example of the linear curve. For the

experiment on this paper, the sensing current is about 5mA and the sensing voltage is near the range of 0.8V. Thus the total joule heating due to one sensing diode is about 4mW. If the thermal resistance of junction to ambient is 0.5K/W, then the impact of the sensing power to the shift of temperature is around 0.5 K/W x 4mW = 0.002 degree which is very small and can be ignored for most of the applications, and this guarantee the accuracy of the measurements.

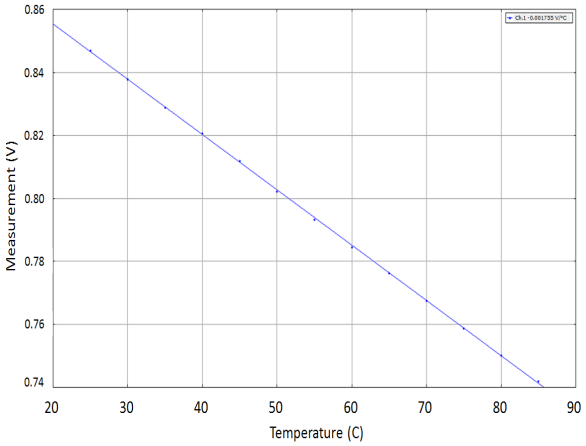

Figure 13. Thermal Sensitivity (K factor) = -1.755mV/K

(5) Results and Discussions

Experimental Rth-JC data (junction to case)

Figure 14 below illustrates one of the result plots of cumulative structure functions. Two different thermal grease materials, one with good and one with bad thermal conductivity, are applied in between cold plate and heat spreader. When the Rth-JC data is lower than ~ 0.2 K/W, the two curves are very close to each other and the separation point could not be clearly seen from the figure. Therefore, the difference of cumulative structure function is calculated, as shown in Figure 15. The Rth-JC here is 0.113K/W. In the real test, several units of the packages are tested to take the average, and the averaged value is about 0.11 K/W. Our data shows that the differences of Rth-JC among units are very small, which proves the measurement technique is very reliable.

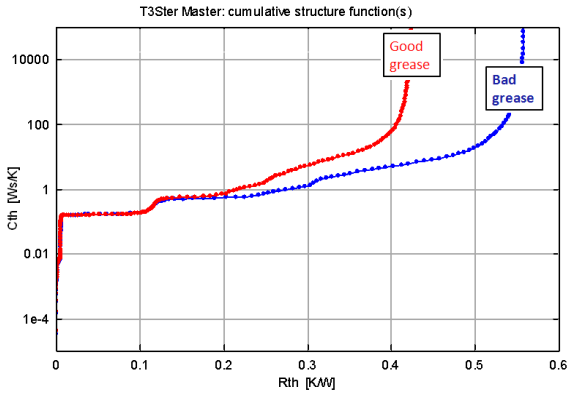

Figure 14. The cumulative structure functions

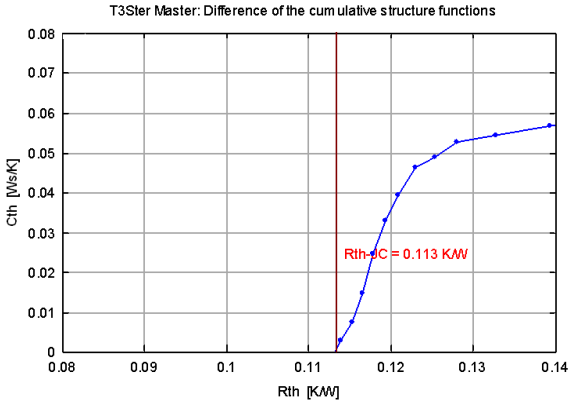

Figure 15. The difference of cumulative structure functions

Experimental Rth-JD data (junction to die)

The Rth-JC has been popularly used because it represents a thermal resistance between the hot spot on the silicon and a point on top of the heat spreader, and the parameter can be used to quickly estimate the temperature of the package. However, the parameter provides little information if we like to know what is the thermal resistance inside the silicon, and what is the thermal resistance coming from the TIM and heat spreader. The inseparable natural of the materials is the main difficulty to obtain such data, but here we propose a new thermal parameter,

Rth-JD

The thermal resistance of junction to die, where the “die” here refers to the top surface of the die, to measure the thermal resistance of the silicon. The approach is explained in the Figure 16 below.

Figure 16 illustrates the traditional method to measure the Rth-JC similar as JEDEC51-14 standard, for which one good and one bad grease materials are used to determine the separation point of the structure functions. The Rth-JC here includes the thermal resistances coming from components of silicon, TIM, and heat spreader. Following the same approach, the left figure, but with the heat spreader is not yet assembled or it is removed after the assembly, the cold plate now is directly attached to the top surface of the silicon, The thermal resistance from the bottom of the die, where is the heating circuits and the spot of junction temperature located, to the top surface of the die is measured.

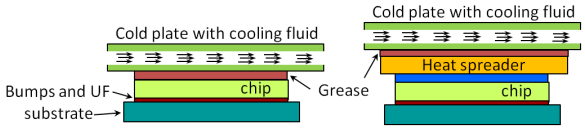

Figure 16. The setup to measure the Rth-JD

Figure 17 illustrates the structure functions of two configurations, with the red curve represents the configuration including the die, TIM, heat spreader, and grease, and the blue curve is the bare die with only the grease material. To clearly locate the separation point, Figure 18 calculates the difference of the structure functions, and the separation point of Rth-JD is around 0.0064K/W. The value is obtained, based on the using when C = 0.0005 Ws/K, the same as getting Rth-JC in the JEDEC 51-14, to calculate the resistance. The thermal conductivity of silicon is very good and its thermal resistance is very small and very difficult to measure, but with current proposed measurement technique, its impact can be studied. The thermal resistance of Rth-JD here includes not only the impact of the material but also the dimension or structure factor, and therefore, it shall be a more appropriate parameter to characterize the thermal performance. With known Rth-JD, the combined thermal resistances of TIM and copper can be calculated from the equation

Rth (TIM + lid spreader) =~ Rth-JC – Rth-JD

and for the study here, the value is 0.116-0.005 = 0.111 C/W. However, based on the experimental analysis so far, the accurate measurement of Rth-JD is still very challenging due to the noise issues. The work is still under development and we propose the concept of Rth-JD for thermal community to consider the approach to study the impacts of components.

For typical flip chip devices, the Rth-JD may be too small to consider, but the proposed technique and parameter here have potential applications such as (a) it provides a method to characterize the thermal resistances of the components of TIM and heat spreader, not including the component of silicon (b) it may be crucial for the next generation packaging devices when the thermal resistance of die has to be addressed (c) it provides a method to characterize the thermal behavior for the multi-dies or stacked dies, such as that the GPU and CPU are coupled together on the coming powerful tablet devices these days (d) it provides a potential technique to study the impact of non-uniform powering of the silicon. The proposed technique is still under researched and developed at STATS ChipPAC and more data are to be published later.

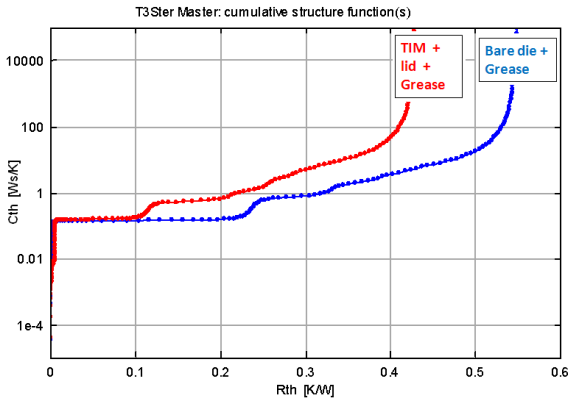

Figure 17. Structure functions of two configurations

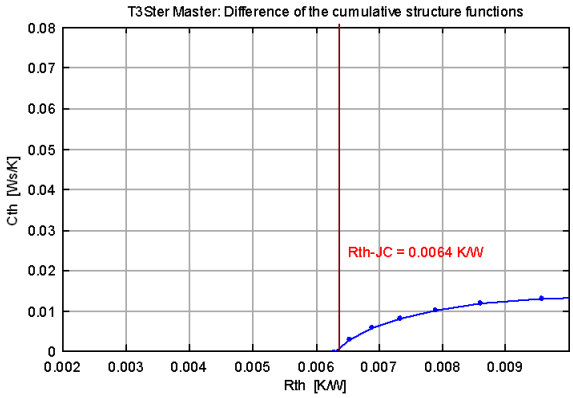

Figure 18. The difference of structure functions

Experimental Rth-JA measurement with a forced convection fan cooling heat sink assembly

The thermal resistance of junction to ambient, Rth-JA, is one of the most important thermal application parameters used in the real final products. To evaluate its impact, a forced convective air cooling heat sink is attached on to the package as shown in the Figure 19. There are 4 screws, not shown in the figure, used to tight the PCB with the heat sink base. A fan with its RPM speed being adjustable is used to vary the air speed and to study the impact of Rth-JA. The fan's RPM is controlled through the applied voltages and Figure 20 illustrates one of the measured Rth-JA data. The higher the applied voltage, the higher the fan speed, and therefore the Rth-JA is the lowest 0.755 K/W, while for applied voltages of 10V and 8 volts, the Rth-JA becomes 0.775 K/W and 0.793 K/W, respectively.

The use of the measurement technique here provides an excellent method to characterize the thermal performance of the heat sink cooling assembly, especially in the real applications. In the real characterization, the heat sink configuration, the fan speed, the grease materials and thicknesses, and fan designs are to be carefully evaluated and designed, and STATS ChipPAC is providing the systematic measurement schemes to support customers.

(6) Conclusions

The conclusions of the paper are listed below: (a) a well-defined, non-ambiguous thermal parameter, Rth-JC is to be re-defined by the thermal community, and we propose Rth-JP which may be a more appropriate parameter to include the spreading effect of the heat dissipation in the heat spreader, so a better correlation with the experiment is possible (b) all the thermal resistance parameters between junction and lid, are in the range of 0.11 to 0.13 K/W, which may be accurate enough for most of the common applications (c) the measurement of thermal resistance of Rth-JD is proposed to characterize the components of silicon, TIM, and lid (d) the thermal resistance of the junction to ambient under different fan operating conditions are measured.

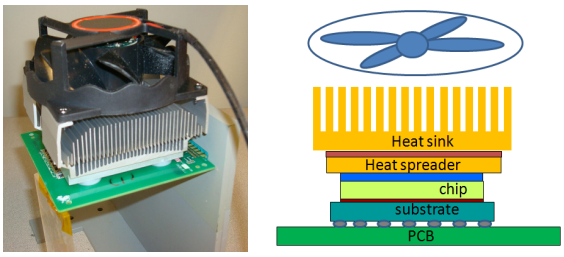

Figure 19. Forced convection fan cooling

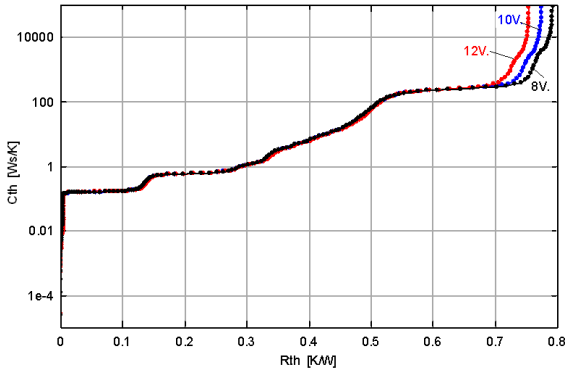

Figure 20. Measurement of thermal resistance of junction to ambient, Rth-JA, with various applied voltages on the fan

(7) Future Works

The ambiguity of the Rth-JC definition and how to come out a more reasonable and useful thermal parameters deserve more research and development for the thermal community. STATS ChipPAC is still working on the following items (a) a better definition of the Rth-JP to consider the impacts of the geometry and thermal spreading resistance for the real applications (b) standardization of the measurement of the thermal resistance of junction-to-die and identification of the resistances of TIM and heat spreader (c) study of the heating of the thermal die with different configurations of resistors, such as parallel and serial connections, and how the structure functions vary due to the power mappings (d) development of the measurement schemes to characterize the silicon thermal resistance especially for the multi-die packed together inside the small packages which could be very crucial for the development of the computer tablets and mobile gadgets (e) the development of the numerical and experimental schemes to define the effective thermal conductivity of TIM layer.

(8) References

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