“Transient Thermal Characterization of a fcBGA-H Device”

by

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Abstract

In this paper, we describe a study in which the thermal performance data of Theta jc (Rth-JC), Theta ja (Rth-JA), and structure functions of a flip-chip ball grid array device with heat spreader, fcBGA-H, was measured. For Rth-JC, various boundary conditions for the thermal resistance modeling were considered and are discussed here. A transient measurement method was used to obtain the temperature responses of the diodes. The structure functions of the diodes were measured; and the thermal resistances were calculated. Furthermore, the effect of power map on the structure functions was studied, and a thermal simulation was conducted to match the simulated structure functions with the experimental structure functions. The matched simulation structure functions provides the most accurate thermal resistor network for system level thermal evaluation.

Keywords

TIM, structure function, thermal resistance, power map, junction temperature, flip chip

1. Introduction

Flip-chip packages are commonly used for various applications such as desktop computers, servers, telecommunications, gaming, etc. Power levels and more importantly die heat-flux densities are drastically increasing because of tremendous demands on die functionality. Thus, customers are constantly pushing packaging industries to lower thermal impedance of thermal interface material (TIM) for very high-power flip-chip packages.

TIMs are thermally conductive materials used to increase the thermal contact conductance across jointed solid surfaces, such as between CPUs and heat spreaders. If there is tiny air gap, which is a very poor conductor, filled at the interfaces with contacted solid surfaces, the efficiency of heat dissipation will be drastically deteriorated. As a result, thermal characterization of the TIM is crucial to meet the thermal specification for reliability, especially the parameters for the highest temperature on the die (Tj), the temperature on the top of the heat spreader (Tc), and the thermal resistances between these two spots or locations [1]. The traditional way of measuring the case temperature (Tc) is to use a thermalcouple at the center of the heat spreader. The major problem with this classical measurement standard is that it requires the case temperature to be at center, but in real applications the location of the hottest point may be unknown, especially when the die is heated with non-uniform power.

The goals of this paper are to (1) describe measurement of TIM thermal performance, especially the Rth-JC, on an assembled flip-chip ball grid array device manufactured at STATS ChipPAC using the transient measurement techniques [2] without the need of a thermocouple; (2) describe measurement of the thermal performances of the packages, Rth-JA, with cooling fans running at different speeds, to simulate the real application conditions; (3) illustrate the effect of a power map on the structure function; (4) describe a thermal simulation to generate a simulated structure function, modify the simulated structure function to match with the measured structure function, and use the modified simulated structure function to generate a thermal resister network for system level applications, and (5) identify and propose better simulation and experimental approaches.

2. Configuration of the Package and Thermal Test Vehicles

A flip-chip test vehicle was built internally at STATS ChipPAC to evaluate the thermal performance of the TIM, and the configuration is shown as in Figure 1. The test package includes the following components, from top to bottom: a 25 x 25 x 1 mm copper heat spreader, TIM layer, silicon chip, a layer of underfill and solder bumps, a 12-layer substrate with total thickness 1.65 mm, an array of solder balls, and a PCB. On the side, the epoxy material is used to bond the copper lid with the substrate.

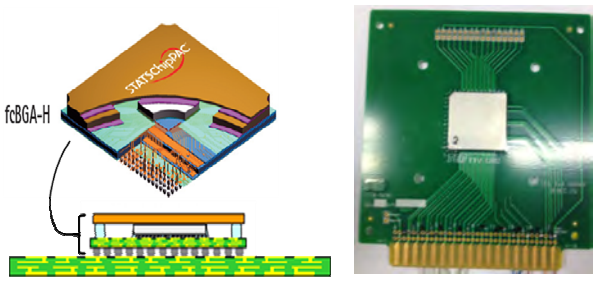


Figure 1. The views of the test vehicles.

The full coverage of TIM on the die was carefully processed, and the thickness of the TIM was monitored and controlled to be around 38 µm with the tolerance smaller than

2 µm, as shown in Figures 2 and 3. The thickness was controlled through the mechanical press applied on top of the heat spreader right after the TIM dispensing and during the curing process.

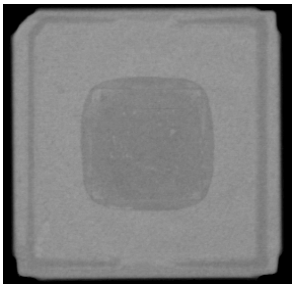


Figure 2. TIM coverage

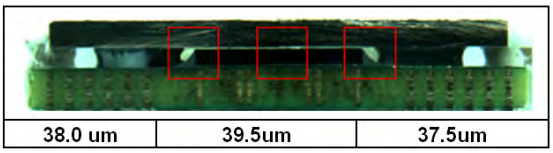


Figure 3. TIM thickness measurements

2.1. Thermal Test Die

Thermal test dies have been widely used in package design qualification. Figure 4 shows the thermal test die, which is 10 x 10 mm, used in this experiment. The die has 4 x 4 = 16 cells, and each cell can be used individually, or some cells can be connected together depending on the needs of the test conditions, such as, uniform heating or non-uniform heating. Ten diode sensors are populated on the die to measure the temperatures either at the center, at the sides, or at the corners. In this test, all the 4 x 4 cells were used to generate uniform heating of the die.

Figure 5 shows that the resistors on each row are connected together. All the row resistors have to be coupled together to power the entire die all together at the same time, and either serial or parallel resistors can be used. However, the serial resistors guarantee a constant electrical current flowing through all the resistors, whereas parallel resistors may cause an unbalance of the current magnitude between the rows of resistors, especially when the length and width of the traces are different. Therefore, the serial resistors were used.

2.2. Calibration of the Diodes

As shown in Figure 4, 10 diodes are populated on the silicon die. The diodes are used for the measurements of the temperatures at various locations. As a small electrical current flows through the diode, the voltage drop across the two ends of the diode is linearly dependent on the temperature. Therefore, before the heating of the package, each diode is calibrated to get its voltage responses as a function of the temperatures, or thermal sensitivity data, and Figure 6 illustrates one example of the linear curve.

For this experiment, the sensing current is about 5 mA and the sensing voltage is near the range of 0.8 V. Thus, the total joule heating caused by one sensing diode is about 4 mW. If the thermal resistance of junction to ambient is 0. 5K/W, then the effect of the sensing power to the shift of temperature is around 0.5 K/W x 4 mW = 0.002 degree, which is very small and can be ignored for most of the applications. This guarantees the accuracy of the measurements.

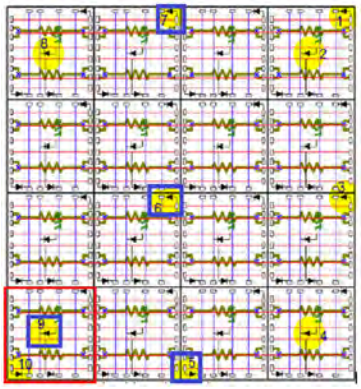


Figure 4. Thermal test die

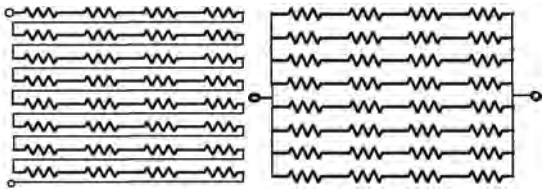


Figure 5. Serial and parallel resistor heater

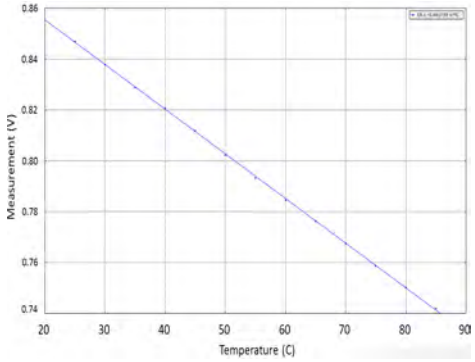


Figure 6. Thermal sensitivity (K factor) = -1.755 mV/K

3. Experimental Setup

We applied the thermal transient measurement approach, as shown in Figure 7, using a commercially available test system to analyze the structure of the devices and to measure the temperature elevation at the selected sensor locations.

The samples were pressed against a liquid cooled cold-plate with a constant pressure of 3 bar. Each sample was heated up by a steady heating current of 325 mA, resulting in approximately 26 W heating power. As soon as the device reached a thermal steady state, the power was switched to the sensor level, maintained by a 5 mA measurement current. The pre-heating phase lasted for 480

seconds, and it took an additional 480 seconds to capture the cooling curve until it reached its final steady state.

Two measurements were taken on each sample: one with thermal grease between the lid and the cold-plate, one without it. Each measurement was converted to structure functions using the Network Identification by Deconvolution (NID) method, and the corresponding measurements were compared to each other. With this method, we could identify the Rth-JC of the samples using a similar approach to the JEDEC JESD 51-14 test method.

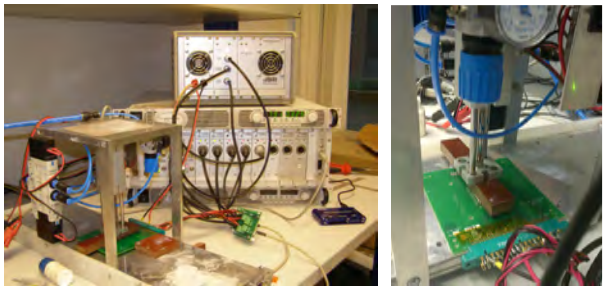


Figure 7. Experimental setup

4. Simulation & Experiment of Rth-JC

The thermal simulation tools have been very popular in the prediction of the thermal performance of the IC packages. The early stage of thermal modeling could help predict the thermal reliability of the IC packages and provide important factors for system-level thermal evaluation and optimization. For lots of situations, instead of real thermal testing, modeling is heavily used to avoid time-consuming and costly experiments. In this section, the thermal resistance of junction-to-case, Rth-JC, which is one of the most important thermal parameters, especially for the flip-chip devices, is numerically studied [3,4,5,6]. But first, several cases of Rth-JC are modeled and compared.

4.1. Fixed Rth-JC vs. Floating Rth-JC

A simple model was built to check the effect of various boundary conditions. The fixed case Rth-JC here refers to the top of the lid which is assumed to be fixed at a constant temperature as shown in Figure 8. For this configuration, the heat dissipation toward the lid top is in vertical or in out-of-plane direction, and it has less in-plane heat spreading inside the lid, while the floating case Rth-JC allows the temperatures on the top of the lid to vary depending on the cold-plate conditions. The location of traditional case temperature, Tc, is shown as in the equation below

$$\text{Rth-JC} = (\text{Tj} - \text{Tc}) / \text{Power}$$

where the Tc refers to the temperature at the top center of the heat spreader.

For the floating Rth-JC, two configurations are considered. The first is a cold plate with a cooling fluid inside, and the second is a cold plate replaced by a similar size of copper block and assuming that the top of the block is kept at a constant temperature. The boundary conditions of the three configurations are shown in Figure 8. The CFD and heat conduction simulation were conducted to calculate the Rth-JC of all the configurations.

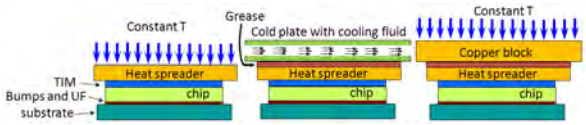


Figure 8. Boundary conditions for Rth-JC modeling, fixed case, cold plate, and copper block

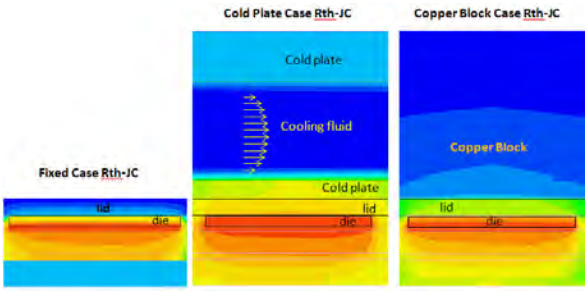


Figure 9. Temperature distributions near the die and lid

Figure 9 illustrates the simulation result of the temperature distributions from the three different configurations, and Table 1 shows the calculated Rth-JC data. The Rth-JC from the fixed case is about 15□20% higher than the ones from the cold plate and copper block. The cold plate configuration is the most comprehensive consideration of the real situation; however, several serial of modeling cases indicate that the copper block case is a quick, simple, and reasonable approximation to obtain more real-world Rth-JC data.

Configuration	Top Lid Surface Temperature	junction T	Case T	Rth-JC
Fixed Case	constant (20C)	20.351	20	0.117
Cold plate	vary by locations	21.712	21.422	0.097
Copper block	vary by locations	20.839	20.537	0.101

Table 1. The thermal resistance data

4.2. Effective Material Properties of TIM

Besides the boundary conditions mentioned in the previous section, the effective material properties of TIM is important, but probably difficult, to determine. The common procedure to determine the true effective thermal conductivity of the TIM layer is to manufacture several test samples with different TIM thicknesses; and from the measurements of the temperatures inside the test samples, the effective thermal conductivities of TIM layers can be plotted as a function of the thicknesses. The disadvantages of the approach are that the thermal conductivity could be very nonlinearly dependent of the thickness and lots of samples may be needed, because of the fluctuation of the test data, to determine the thickness-conductivity relationship.

In our study, the TIM thickness over 50 μm was not permitted because of the thermal budget of the device. Therefore, all the thicknesses of the packages are controlled

near 38 µm, without other different experimental TIM thicknesses to estimate the effective thermal conductivity of the TIM layer as a function of the thickness. The determination of the effective conductivity of TIM must rely on the single available thickness in the experiment.

To do so, we proposed the calculation scheme shown in Figure 8. Initially, a thermal conductivity of TIM layer is assumed to simulate the Rth-JC of the device when compared with the experimental Rth-JC. When the difference (Δ) is larger than the spec (S), another different of the thermal conductivity of TIM layer is assumed and repeated. The iteration keeps going until the tolerance is met. In this study, we found that the effective thermal conductivity was different from the given data provided by the TIM vendors.

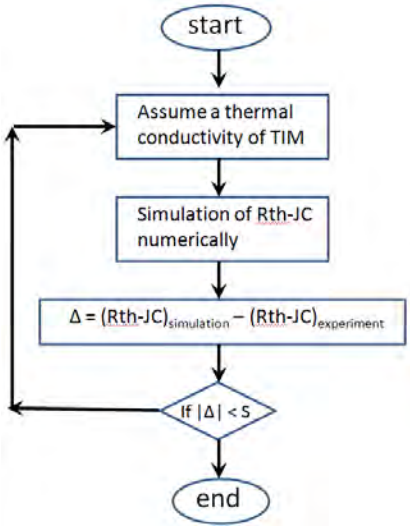


Figure 10. The simulation scheme to determine effective material properties of TIM

The procedures here introduce a method to obtain the effective material properties of TIM. This approach is based on a steady state 3D thermal simulation, without the need to know the transient response behaviors of the package. The power density was assumed to be uniform for this case. The obtained data of Rth-JC may be enough for some industrial's applications but basically the approach is not fully in accord with the physics of JEDEC 51-14, which uses transient approach in principle. The transient approaches, in theory, may provide more insight of a package's thermal behaviors. Thus, section 5 describes implementing a transient approach.

4.3. Measurement of Rth-JC

Using the experimental setup as mentioned in section 3, Figure 11 illustrates one of the result plots of cumulative structure functions. Two different thermal grease materials, one with good and one with bad thermal conductivity, are applied in between the cold plate and heat spreader. For the Rth-JC data, less than ~0.2 K/W, the two curves are very close to each other and the separation point could not be clearly seen. Therefore, the difference of cumulative structure function was calculated, as shown in Figure 12. The Rth-JC here is 0.113K/W. In the real test, several units of the packages were tested to take the average, and the averaged value was about 0.11 K/W. Our data shows that the differences of Rth-JC among units are very small, which proves the measurement technique is reliable.

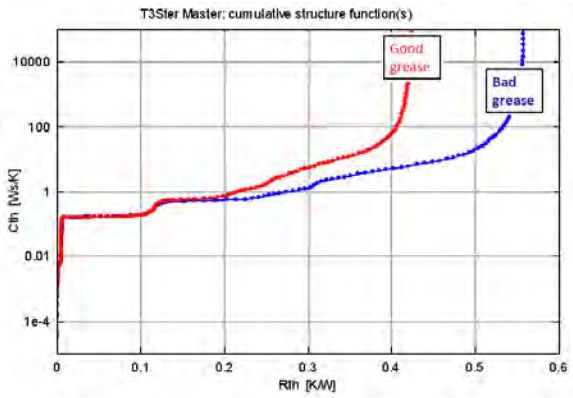


Figure 11. The cumulative SFs

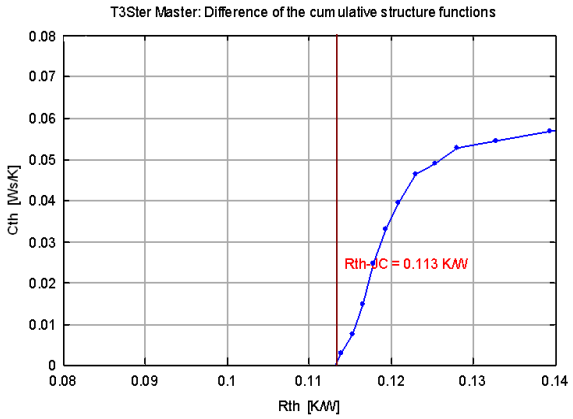


Figure 12. The difference of cumulative structure functions

5. Thermal Characterization with Transient Approach

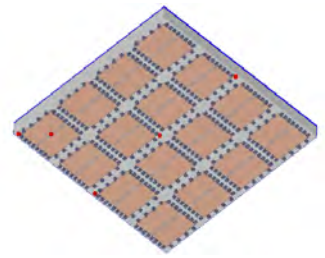
This section describes the transient modeling approach that was usedand the approach was to try and match as detailed as possible with the real measurement conditions. The local temperature response of diodes is strongly affected by the thermal conductivity, capacitance, dimension, configuration, and power map. Thus, all the parameters were taken into account in the simulation to better match experimental data.

5.1 Transient Modeling

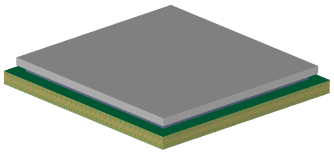
After the determination of the effective material properties of TIM, as mentioned in the previous section, a full 3D thermal package model was constructed (Figure 13) for the transient modeling. The model considered as much as possible the detailed features, such as the solder bumps, heating resistors, underfill, substrate layers, solder balls, PCB layouts, Nylon block, epoxy lid attach material, power maps, and the locations of thermal diodes.

In theory, if a steady state simulation is conducted, the obtained Rth-JC data would be same as described in the previous section. However, the detailed configuration was

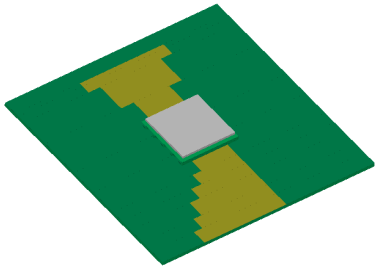
more appropriate for transient thermal characterization because all the detailed features effect the temperature response of diodes. Figure 13a illustrates a bottom view of silicon chip with solder bumps and underfill. Figure 13b is the top view of the silicon sitting on a substrate, and all the substrate layers were considered and included in the simulation. Figure 13c shows the package surface mounted on a PCB with solder balls, and all the solder balls were modeled as well. Figure 13d illustrates the flipped assembly, with the chip surface facing a cold plate; a thermal grease may be used for better contact. A rectangular Nylon block was on top to press a force and to control the thickness of thermal grease.



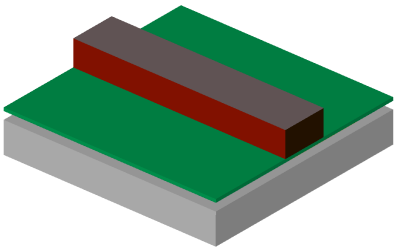
(a) Bottom view of silicon chip with solder bumps



(b) Top view of silicon chip on the substrate



(c) Package is mounted on a PCB



(d) Thermal test vehicle is flipped for experiment

Figure 13. Simulation considering all detailed features

5.2 Effect of Power Map on the Structure Function

The accurately measured SF shown in this paper can eliminate the material uncertainties caused by either data from different vendors or from inconsistent manufacture processes. The highly precise structure function is able to identify these variations. The hardware used, T3Ster™, can capture multiple sensor diodes at the same time with about 1□10 µs sample rate. However, besides the material and structure variations, the power map may affect the structure functions as well. In this section, some data are demonstrated below. The test chip used in this experiment contained 16 cells with 10 sensor diodes on it. There is a pair of resistor heaters as shown in Figure 14; the two blocks on each cell do the heating.

The four sensor diodes 5, 6, 7, and 9 were chosen for this study because of their representative locations. Sensor diode 6 is located near the center of the silicon, and its measured temperature, Tj, was used for the Rth-JC calculation.Sensor diodes 5 and 7 are located at the edge of the silicon, and sensor diode 9 is located at the center of bottom left cell, and it is exactly at the center in between two resistor heaters. Furthermore, the distances of diodes 5, 7, and 9 to their respective heating resistors are about the same.

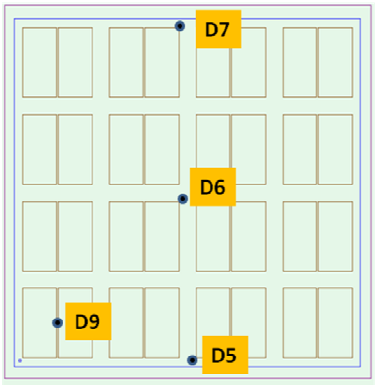


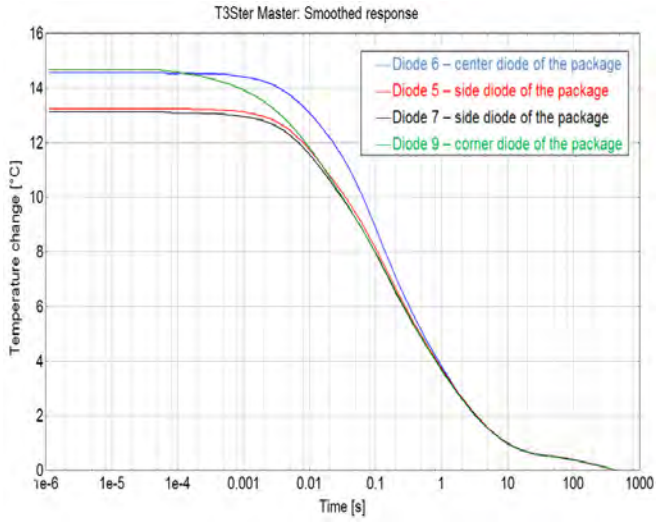
Figure 14. the locations of sensing diodes

The captured thermal transient temperature response curves of the four sensor diodes are shown in Figure 15a. The plot clearly shows the responses of temperatures are different among sensor diodes. The temperatures are offset to the same value to better compare the differences, as shown in Figure 15b, so the diodes' response rates can be easily checked. Sensor diode 9, which is located in between two heating resistors, has the quickest response time, approximately 400 µs ahead of other sensor diodes. Sensor diodes 5 and 7 are located at the silicon edge; and because their distances to the resistors are about the same, they have the same temperature response curves. Sensor diodes 6 and 9 have about the same total temperature change but the shapes of their temperature response curves are different because of the variation of capacitances that the diodes experience from the outside environment.

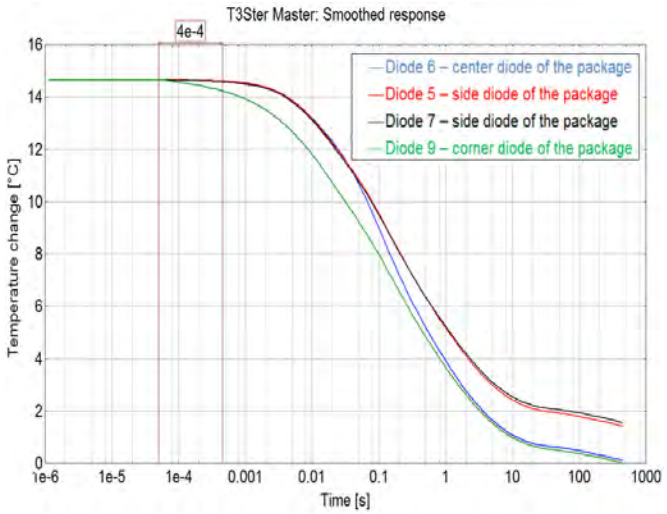
The differences of the temperature response curves or the propagation delays, for this study, are caused by (1) the relative distances between the sensor diodes and heating resistors, which is related to the "heating source" capacitance, and (2) the "structure" capacitance each diode experiences from the device's configuration and materials. The effects of

these two parameters are summed up together and not separated in the figures.

The captured transient temperature response curves were fed into the T3SterMaster tool, which uses the Network Identification by Deconvolution (NID) method, to generate structure functions. Structure function plots, namely, the plots of thermal capacitances vs. thermal resistance, are extracted from T3SterMaster, as shown in Figure 16. Instead of a delta temperature curve, structure functions provide a RC-network showing how the heat is dissipated out of the package. For the Rth-JC measurement, because the heat is dissipated in one direction toward the cold plate, the structure functions provides the detailed information, including the material properties and dimensional variations from the silicon to cold plate.



(a) Experimental temperature response curves without offset



(b) Experimental temperature response curves with offset

Figure 15. Temperature response curves

Figure 16 illustrates that sensor diode 9 has the quickest response time or lowest capacitance as explained above. Sensor diode 9 was ultimately chosen for the study of the correlation, in the next section, in between simulated structure functions and experimental structure functions because it is closest to heating resistors and has the shortest propagation delay. For a device with several diodes and if the distances from diodes to heaters are different, we recommend using similar diodes to conduct structure analysis and model calibration.

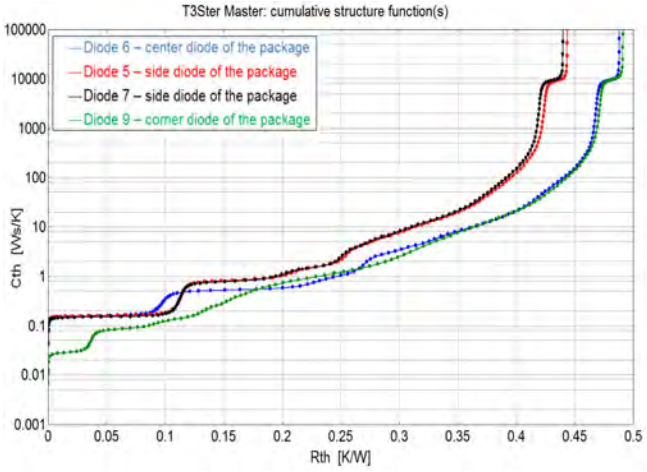


Figure 16. Experimental structure function curves

There are some potential applications of the study of power map on the structure functions, and the work is still ongoing by the authors. One example is mobile handheld devices, for which the temperature response as a function of time could be very important. Another case is the development of multi-chip or multi-core processors because the effect of power distribution on the temperature responses may influence their electrical performances. A better understanding of the relationship of power, temperature, and time is definitely crucial for the next generation of IC design and manufacturing.

5.3. Matching Simulated Structure Functions with Experimental Structure Functions

All previous sections presented experimental temperature response curves and structure functions. This section describes a 3D transient simulation that was conducted to obtain the temperature response of diode 6. The temperature response curve was processed, constructed, and converted to "simulated" structure functions. Like typical thermal modeling, the simulated structure functions may not perfectly match well with the real measured structure function data. The mismatch is caused by either uncertainties of material properties, or the difficulties of simulating all small features and parts on the device, or even the unclear definition of the power map. The good thing is that the simulated structure functions may be calibrated to match with experimental structure functions.

First, a detailed 3D thermal package model was simulated to do the calibration, and the resulting diode temperature vs. time data was processed in T3SterMaster to create the

baseline simulatedstructure functions. The second step was to make a perturbation to the 3D thermal package model and re-derive the structure functions. The third step was to compare the differences between new derived structure functions and experimental structure functions. By perturbing the 3D thermal package model several times and through several iterations, the final calibrated simulated structure functions may match well with the experimental structure functions. The important key of this calibration approach is to identify which parameter needs to be perturbed to get the better matched structure functions. In this study, we perturbed the heat source size on silicon and the thermal resistance of TIM and thermal grease for matching.

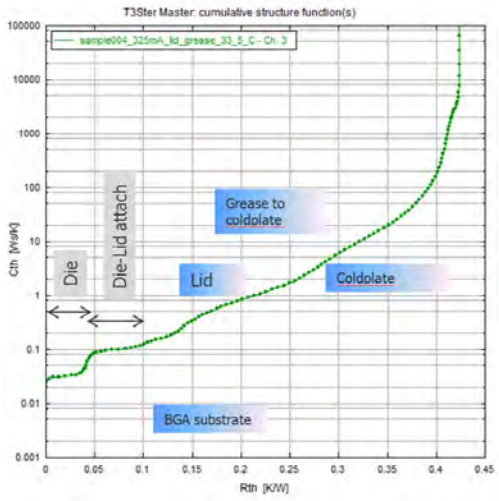


Figure 17. Baseline simulated structure functions in integral form

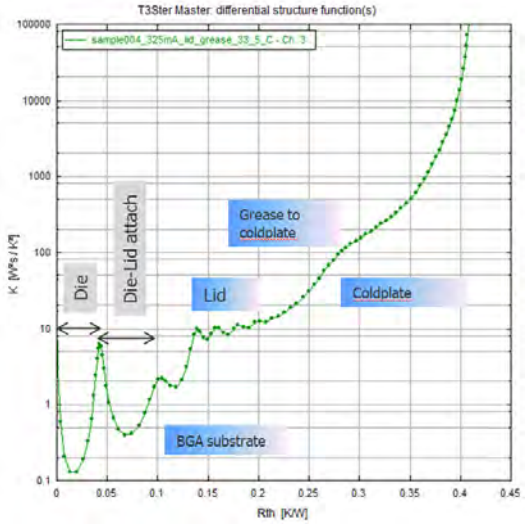


Figure 18. Baseline simulated structure functions in differential form

Figures 17 and 18 shows the baseline simulated structure function in integral and differential forms. Figure 19 shows a big difference between experimental structure functions and the first simulated structure functions, which is called the baseline simulated structure functions here. The difference can be as high as 30□40% and it is caused by many factors mentioned earlier. The big gap between simulation and experimental must be addressed if an accurate prediction is needed, especially if the data is for system level thermal evaluation.

We started from the die region to calibrate the simulated structure functions, and worked outward to perturb various variables to make the simulated structure functions better match the experimental structure functions. Figure 20 shows perturbation of the heat source shapes and size, and the model explicitly considers all the solder bumps and underfill. Figure 21 shows the model calibrated with a higher thermal resistance of TIM material, and Figure 22 shows a lower thermal resistance of thermal grease in between the lid and cold plate. Figure 23 illustrates that the final calibrated simulated structure functions, which were obtained through several iterations, match very well with the experimental structure functions; but there is a mismatch of the two lines at the region where thermal resistance is in between 0.3 and 0.4 K/W. The mismatch is caused by the cold plate's heat spreading effect, which is beyond the concerns of the package. Thus, the calibration process did not continue forward. The final matched simulated structure functions accurately reflect the real resulting thermal impedance of the package, from diode to cold plate.

The ultimate goal of this s study was to use the final calibrated simulated structure functions to generate a Delphi model for system level thermal evaluation. One advantage of this approach is that the measured structure functions are very precise, and the generated Delphi model based on the calibrated structure functions guarantees a precise and real model perfectly matching with the real-world conditions. Furthermore, the calibrated matched structure functions follows step-by-step all of the real heat dissipation paths, which is supposed to be the most accurate approach to generate a Delphi compact model.

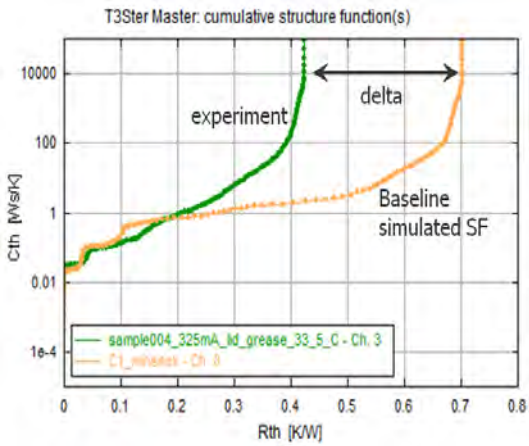


Figure 19. Experimental structure functions and baseline simulated structure functions

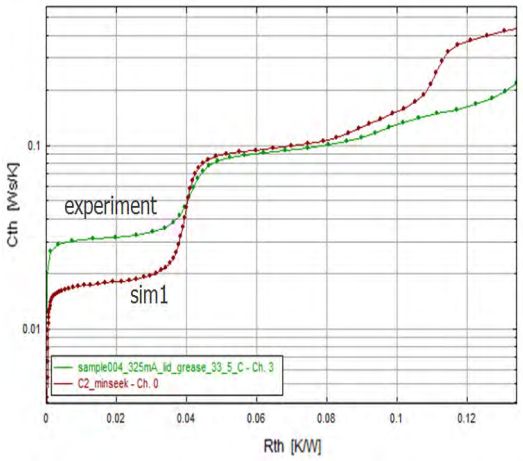


Figure 20. Experimental structure functions and baseline simulated structure functions near die region

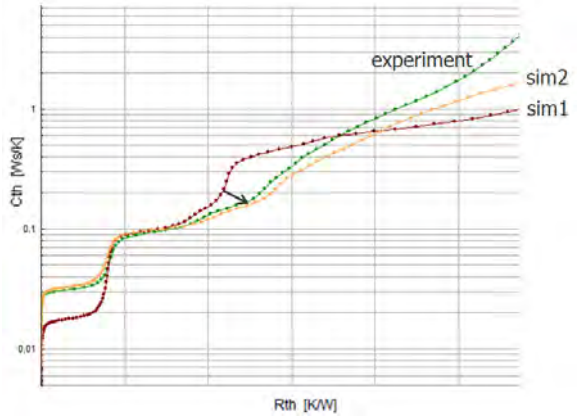


Figure 21. Experimental structure functions and calibrated simulated structure functions

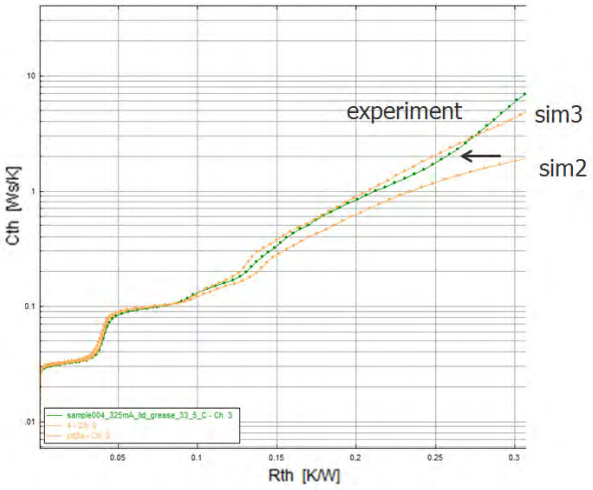


Figure 22. Experimental structure functions and calibrated simulated SFs structure functions

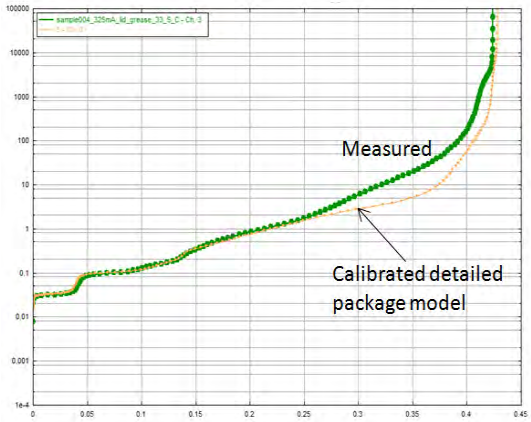


Figure 23. Experimental structure functions and final calibrated simulated structure functions

6. Measurement of Rth-JA with a Forced Convection Fan

The thermal resistance of junction to ambient, Rth-JA, is one of the most important thermal application parameters used in real final products. a forced convective air cooling heatsink was attached on to the package to evaluate its effect (Figure 24). There are four screws, not shown in the figure, that were used to tighten the PCB with the heatsink base. A fan with adjustable RPM speed was used to vary the air speed and to study the effect of Rth-JA. The fan's RPM was controlled through the applied voltages, and Figure 25 illustrates one of the measured Rth-JA data. The higher the applied voltage, the higher the fan speed; therefore, the Rth-JA is the lowest 0.755 K/W. For applied voltages of 10 V and 8 V the Rth-JA was 0.775 K/W and 0.793 K/W, respectively.

The use of the measurement technique described here provides an excellent method to characterize the thermal performance of the heatsink cooling assembly, especially in real applications. In the real characterization, the heatsink configuration, the fan speed, the grease materials and thicknesses, and fan designs need to be carefully evaluated and designed, and STATS ChipPAC is providing the systematic measurement schemes to support customers.

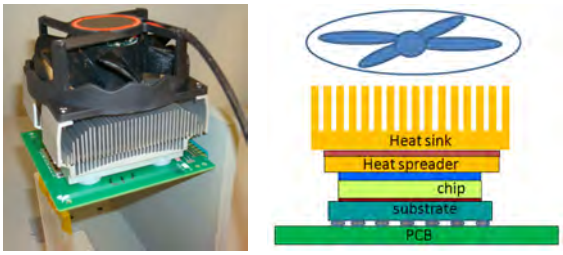


Figure 24. Forced convection fan cooling

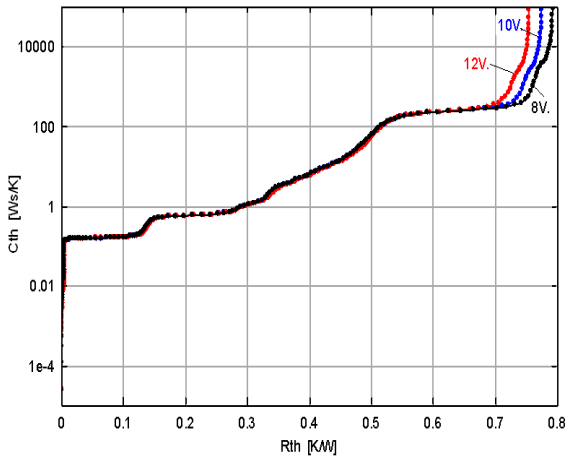


Figure 25. Measurement of thermal resistance of junction to ambient, Rth-JA, with various applied voltages on the fan

7. Conclusion and Future Work

In conclusion, this paper demonstrates the data and capabilities of (1) the simulation and measurement of Rth-JC, (2) the measurement of Rth-JA, (3) the transient responses of devices, and (4) the procedures to generate Delphi model. The authors are still working on the following items: (a) a better simulation scheme to better consider the impacts of the geometry and material properties for Rth-JC standard, (b) automation of the generation of structure function for Delphi model, (c) more transient behaviors of the package, and (d) development of the measurement schemes for multi-die and multi-processor packages.

8. References

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