

Dynamic thermal multiport modeling of IC packages

M. Rencz¹, V. Székely²

¹MicReD Microelectronics Research and Development Ltd.

²Budapest University of Technology and Economics

rencz@micred.com

Abstract

The dynamic thermal behaviour of electronic subsystems is characterised by their dynamic compact models. These models have to be similar to the steady state models in describing the fact that the heat is usually leaving on different locations (ports), necessitating multi-port description of the thermal behaviour. In our paper we present a method suitable for direct generation of multi-port dynamic compact thermal models from a series of thermal transient simulations or measurements. The generated RC electrical equivalent circuit model, exercised with a network simulator program provided the same transient functions as the measured ones for various boundary conditions, proving the accuracy of the method.

1. Introduction

The latest challenge in the field of thermal characterization is the generation of dynamic compact thermal models of the packages. The necessary data may be obtained either from simulations or from measurements. Our main goal was to find a methodology for the automated generation of multi-port models from thermal transient measurements. In these measurements a dissipation step is applied to (or switched off from) the test chip mounted into the package and the temperature response of the chip is recorded. Using sophisticated evaluation methods the compact model of the package can be extracted from these responses. The evaluation of the recorded responses is a question that has challenged many researchers for the last two decades – see e.g. [1], [2], [3], [4].

There are two characteristically different ways for model identification from the obtained transient curves. The one that is followed by most of the research groups is the ad-hoc generation of the model structure, and fitting the parameters to the measured results by usual curve fitting methods.

The method described in [2] is the only generic method presented: this is the direct transformation of the heating or cooling curves and identification of the time constants of the response function by the NID (Network Identification by Deconvolution) method.

This methodology works quite well if the generation of "one-port" models is intended only. In other words: if the thermal boundary conditions are fixed around the package, and the heat flows according to a fixed streaming pattern from the chip towards the boundaries. Such a model is valid strictly only for the

boundary conditions of the measurement from which it was identified. Changing the boundary conditions will result in new measured heating or cooling curves, consequently new model parameters of the identified models.

Assuming multiple locations where the heat can leave the system, that means, multiple terminals, the package has to be considered as a *thermal multi-port*. Having multi-port models the effect of applying different boundary conditions may be also considered – at least for the boundaries that are considered as "ports" in the model.

Several authors recognized this earlier; a good summary of these papers can be found e.g. in [5]. Reports of recent results in this field can be found in [6] and [7]. These authors however discuss the issue of multi-port thermal modeling only in steady state conditions.

Data acquired from multi-port thermal transient measurements are the basis of multi-port, dynamic compact model generation. For the identification of such multi-port models heuristic approaches are already known in the literature (see e.g. [8]), but we are targeting a more generic approach. Our initial trials in this field were already briefly described in [9].

In developing the generic methodology the first step is to define the general form of the model, this is described in the first part of the paper. The second part discusses the special questions of obtaining models from measurements.

2. Theoretical background, the generic model

The base of our model generation methodology is the frequency domain description of multi-ports with y parameters. For electrical two-ports this description looks as follows:

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \cdot \begin{bmatrix} u_1 \\ u_2 \end{bmatrix}, \quad (1)$$

where the i and u values refer to the electrical current and voltage values respectively.

An analogous description can be used for the description of thermal multiports, where p designates the amplitude of the frequency dependent heat currents and τ gives the amplitude of the frequency dependent temperatures. For a 2-port case this leads to the following equation:

$$\begin{bmatrix} p_1 \\ p_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \cdot \begin{bmatrix} \tau_1 \\ \tau_2 \end{bmatrix}. \quad (2)$$

The y electrical or thermal admittance parameter values are complex valued in both cases. Knowing the y values in the function of frequency we have an appropriate model of the time dependent behavior, either in the electrical, or in the thermal domain. If the $y_{ij}(\omega)$ functions are available in the form of algebraic equations we have obtained a behavioural model of the two-port, if they are available in the form of circuit elements we have an equivalent circuit model. In this latter case the individual y admittances still have to be connected with the help of controlled sources in order to form a complete model, e.g. according to Fig. 1.

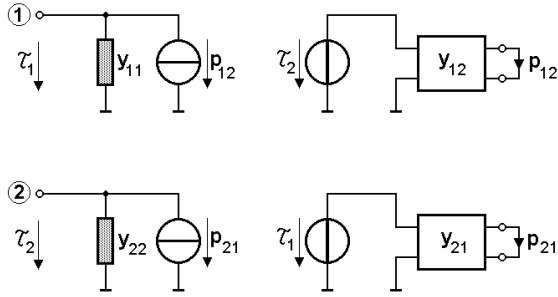


Fig. 1. A model network to realise Eq. (2)

From now on we deal only with model generation in the thermal domain. To have an appropriate model of the thermal behavior of e.g. a package we need to know the complex thermal admittances in the function of the frequency.

To demonstrate the characteristics features of the admittance functions in the thermal domain let us investigate the thermal y two-port parameters of a homogeneous rod of uniform thickness. The two ports are the back and front ends of the rod, see Fig 2. The y parameters of this symmetrical structure can be calculated as follows [10]:

$$y_{11} = y_{22} = \sqrt{\frac{sc}{r}} \coth(\sqrt{src} L) \quad (3)$$

$$y_{12} = y_{21} = -\sqrt{\frac{sc}{r}} \frac{1}{\sinh(\sqrt{src} L)} \quad (4)$$

– where r is the thermal resistance per unit length, c is the heat capacity per unit length, L is the length of the rod and $s = j\omega$ is the complex frequency.

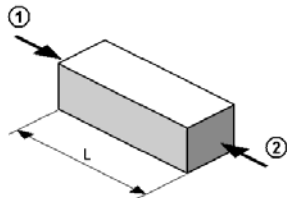


Fig. 2. A simple example of a thermal two-port

Let us aim at developing a network model. In this case we have to find an appropriate lumped approximation of the ω dependent thermal admittances in the form of e.g. RC ladder networks.

The main diagonal elements of the admittance matrix

(y_{11} y_{22} , etc) are driving point admittances. In case of thermal structures, characterized by node-to-node resistances and node-to-ground capacitances in the finite difference model of the distributed structure, the driving point admittances always start from a finite ohmic value. With increasing frequencies they become complex and their absolute value keeps to the infinite. This can be seen in Fig. 3. as well, where the $y_{11}(\omega)$ admittance of the homogeneous thermal rod is depicted.

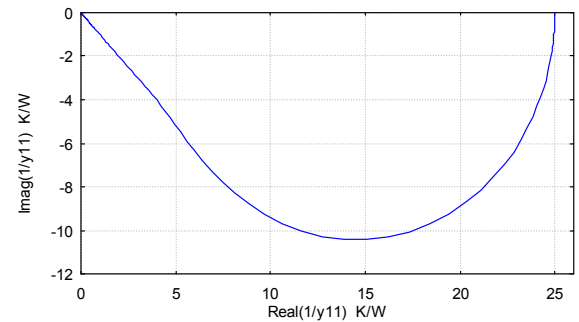
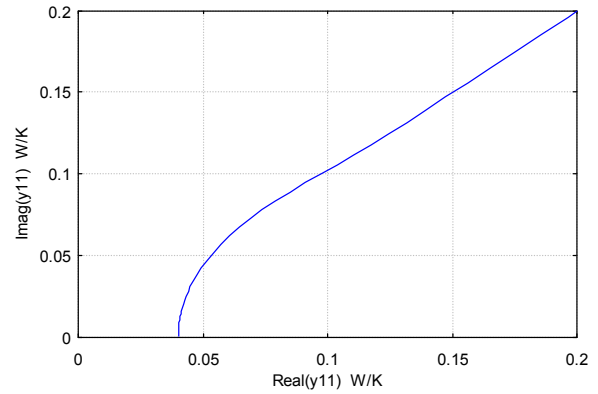


Fig. 3. The $y_{11}(\omega)$ thermal admittance function of the homogeneous heat conducting copper rod of 10mm length and 1mm^2 cross section area. (a) presents the complex locus of the admittance function, (b) presents the complex locus of the thermal impedance function.

In case of main diagonal elements the reciprocal of the y matrix elements, e.g. the $z_{ii} = 1/y_{ii}$, driving point impedances with shorted other ports are more convenient to be modeled, since they do not have parts that tend to the infinite. They start from real values, continue with complex values of positive real and negative imaginary parts and tend to the origin with a 45° phase angle in case of $\omega \rightarrow \infty$. The 45° phase angle for high frequencies is a characteristic feature of port impedances of distributed systems. Such impedances are usually modelled with RC ladder networks of Fig.4a. Commercial identification programs are available (e.g. THERMODEL-f) to calculate the elements of the ladder network from the impedance function. [11] The number of the ladder stages depends on the required accuracy.

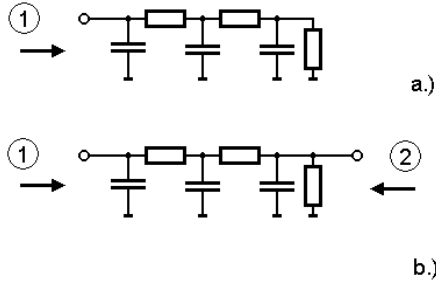


Fig. 4. One-port and two-port RC ladder networks to model driving point and transfer impedances

The further elements of the y matrix, that is, the elements out of the main diagonal are the so-called transfer admittances. Their shape is usually different from the shape of the driving point admittances. They start from negative real values and with increasing frequencies their imaginary part first becomes positive. Their absolute value diminishes and tends finally to 0 with increasing frequencies, while its phase angle increases well over 180° and more, turning around the origin. Thermal transfer functions showing a phase angle higher than 90° have to be modeled with two-port ladder circuits of Fig. 4.b.

These characteristic features are well observable on the $y_{12}(\omega)=y_{21}(\omega)$ admittance locus of our previous example, the homogeneous heat conducting rod of Eq. (4). Fig.5. shows this function.

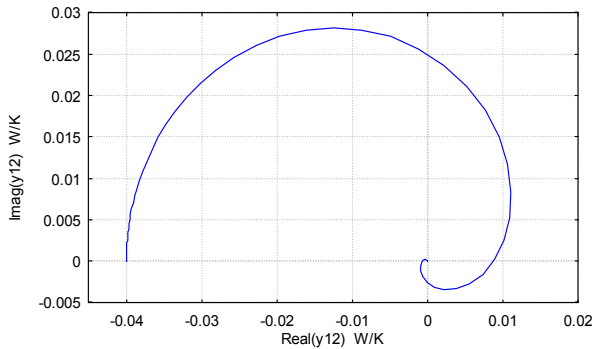


Fig 5. The $y_{12}(\omega)=y_{21}(\omega)$ thermal transfer admittance functions of the homogeneous heat conducting rod of Eq. (4). The values are calculated for a copper rod of 10mm length and 1mm^2 cross section area.

The proposed form of the generic model is shown in Fig. 6. In this model network the y_{12} and y_{21} transfer admittances are modeled by the transfer impedance of the corresponding ladder networks. This allows us to couple the transfer impedance models with VCCS (voltage controlled current source) elements. This way, only one type of controlled sources has to be used, which holds some ease during the model implementation. The g_m transconductances of the controlled sources can be chosen as unity: 1 W/K. Obviously the length of the four RC ladders may be different. If 1 is the cavity-side port of the package, it

is advantageous to select a 4 or 5 stage model for y_{11} in order to represent the behavior of the near-chip region. For the other admittances one or two stage ladders may be sufficient.

The network functions of the RC ladders representing y_{12} and y_{21} in Fig. 6. have only poles, without zeros. In the case of package problems this is usually enough. If, however, we have to model transfer impedances having one or more zeros as well, the modeling remains still possible. As long as the zeros lie on the negative real axis of the complex frequency plane the modeling with a ladder type RC network is still possible but the network will be a bit more complex.

The presented form of the dynamic two-port model can be extended for 3 or even more thermal ports in a straightforward way.

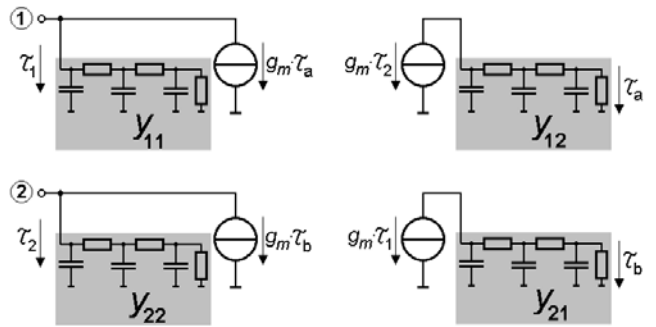


Fig.6.. General form of a 2-port model network. The transfer admittances are realized with impedance functions, coupled to the other parts of the model circuit by VCCS pairs.

We have examined the characteristics of the y loci in case of more complex structures with simulations. Fig.7. presents the investigated structure in the problem definition phase of a SUNRED [11] simulation. 3 ports will be considered: the first one is the middle of the dissipating surface on the top of the chip, the 2nd one is the bottom of the metal mounting platform of the package, the 3rd one is in the middle of the top of the mould. The frequency dependent behavior will be calculated for these ports.

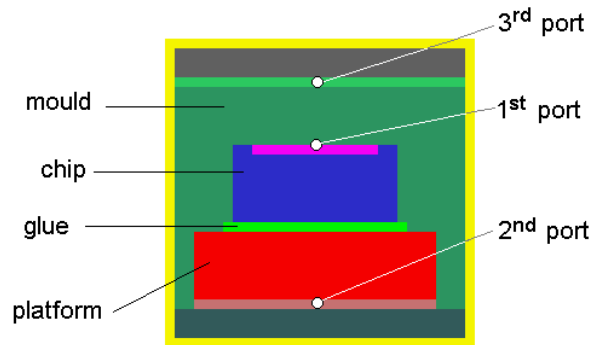


Fig.7. The investigated package structure and the considered ports in SUNRED simulation .

During the simulations we have considered open ports while successively applied dissipation on the different ports and calculated the temperatures on all the ports in the function of the frequency. This way we have

calculated the thermal impedance matrix of the structure. Inverting this we obtained the admittance matrix, see Fig. 8.

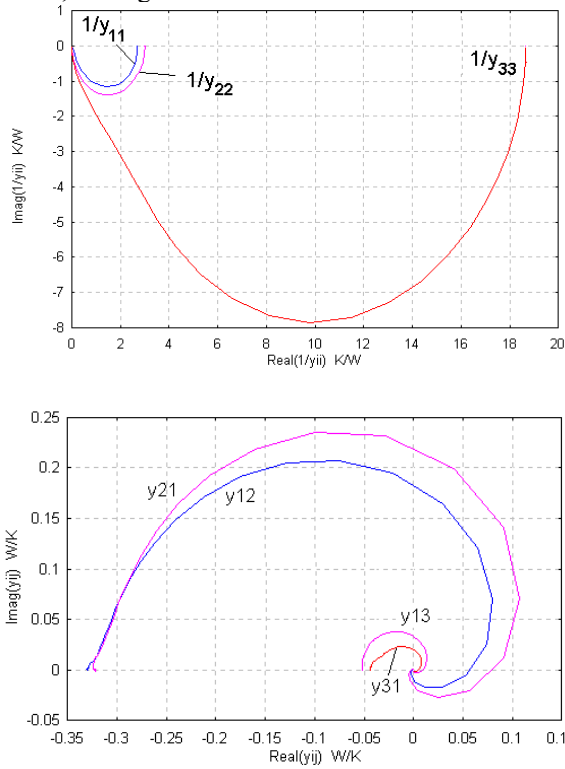


Fig. 8. 3-port admittance diagrams of a package obtained by simulation

As it is visible from the figure the shape of the curves, in accordance to our expectations, are similar to that of the simplest heat conducting rod, presented in Figs 3 and 5. We have to note however that the definition of “ports” holds some ambiguity in this analysis. The dissipating areas have a finite extension, but their temperatures were represented by only one value (in the center point of the port area). Therefore the calculation of the y_{12} and y_{21} and the y_{13} and y_{31} functions that are theoretically the same resulted in slightly different curves, but of course similar in shape. Such curves may be modeled via the THERMODEL tool with RC ladder networks, and be built into the general model network of Fig.6.

This way we have established a methodology for the calculation of generic models, based either on simulation or measurement. The RC ladders may be of course expressed by rational fraction functions as well, resulting in a behavioral type model of the package thermal properties.

3. Measuring thermal multi-port parameters

If we intend to obtain multi-port models from measurements the thermal transient responses have to be recorded for a number of thermal boundary conditions on the various ports of the package [12].

If we use the electrical analogy of the thermal

conduction, the situation is similar to the one presented in Fig.9.

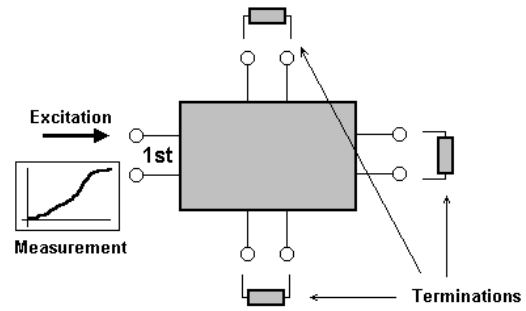


Fig.9. A method for the identification of a multi-port: both the excitation and the measurement are done on the primary port while the terminations on the further ports are varied

The straightforward way were to apply excitation and measurement on all the ports. But since on all the other ports than the chip itself both the excitation and the measurement are rather difficult [13] we try to use only the port where it is easy to apply excitation and perform measurement. This port is the "junction", that is the chip or the thermal test chip in the package. In order to obtain information about the other ports as well, the responses have to be recorded for a number of thermal boundary conditions on the other ports of the structure.

Applying measurements only on the 1st port while the terminations are varied in a prescribed way on the other ports may lead to the identification of the behavior of an electrical multi-port in such a case. Our goal is to find a sequence of measurements in which neither measurement nor excitation is applied on the further ports. Based on such measurements the identification of the model is theoretically possible, though rather ill conditioned. To find out how serious are the practical difficulties in the calculation, stemming from the ill-conditioned nature of the problem we have investigated this approach in details, including feasibility checking and the experimentation of the limits. In this section the results of this research work are presented.

The investigated package was a power IC package from ST Microelectronics. The bottom side of the molded, brick-like package is a metal surface expected to be in good thermal contact with a heat sink. The package offers itself to be considered as a thermal three-port. The ports are J,B,T referring to the junction, the bottom and top surface of the package.

The measurement arrangement is shown in Fig. 10. The package has been mounted in a dual cold plate (DCP) [14] arrangement. The temperature of the DCP mount has been stabilized using the circulating water of the Cole-Parmer Polystat 12100-25 type thermostat. The T3Ster thermal transient tester [11] was used for heating and for recording the temperature responses.

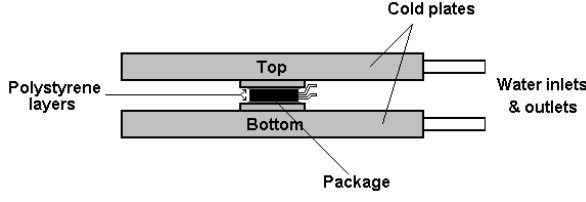


Fig. 10. The measuring arrangement and the thermal boundary conditions

The different terminations were realized by using polystyrene film layers of different thickness. In order to reduce the ambiguity originated from the interface resistance, all surfaces have been coated by heat-conducting grease. The used thickness values are tabulated in Table 1. If the thermal resistance of the thinnest layer is represented by R_{ps} then the resistance of the thicker layers can be expressed with this value as $k \cdot R_{ps}$, where the k coefficients are given in Table 1 as well.

Table 1.

Index	0	1	2	3	4
Thickn ess	(no layer)	100 μm	175 μm	250 μm	500 μm
k	0	1	1.75	2.5	5

A set of the measured responses is presented in Fig. 11. The labels of the curves are the indices of the polystyrene layers: B1T0 refers to the 1st layer on the bottom side and no layers on the top interface. The curves refer to the dissipation step of 15 W.

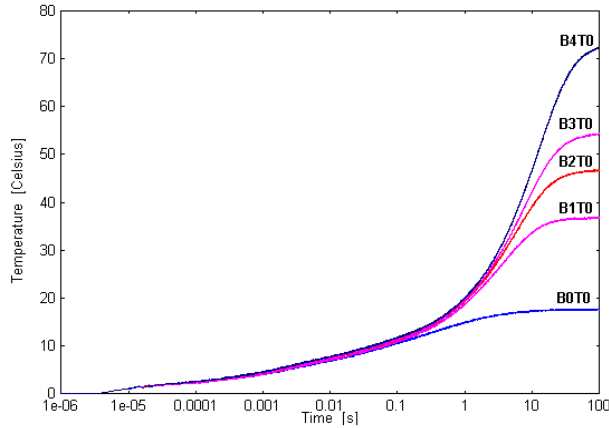


Fig. 11. Thermal responses measured for different boundary conditions

The static thermal resistance values can be easily read from these curves. These values are tabulated in Table 2. For further convenience the thermal conductivity values are calculated as well.

Table 2.

	B0T0	B1T0	B2T0	B3T0	B4T0
$R_{th} K/W$	1.17	2.45	3.11	3.61	4.82

$G_{th} W/K$	0.852	0.408	0.321	0.277	0.207
--------------	-------	-------	-------	-------	-------

4. Evaluation of the results

To any further calculation we need to know the exact R_{ps} values of the polystyrene layers, designated as $k \cdot R_{ps}$. To determine these values the thermal conductivity of $\lambda=0.13$ W/mK was used [15]. The bottom surface of the package is 15×28 mm. These data give for the thermal resistance value of the polystyrene layer of $100 \mu\text{m}$ thickness

$$R_{ps} = \frac{1}{\lambda} \frac{d}{A} = \frac{1}{0.13} \frac{10^{-4}}{15 \cdot 28 \cdot 10^{-6}} = 1.83 K/W \quad (5)$$

If we know the R_{ps} value the elements of the conductance matrix can be determined.

4.1. Calculation of the steady state values

The transient measurement can be used of course also to obtain steady state values. In this section we present how the elements of a steady state, 3 port, boundary-condition independent model can be determined from the measured results [16].

The static linear three-port equation of the package can be written as

$$\begin{bmatrix} P_J \\ P_B \\ P_T \end{bmatrix} = \begin{bmatrix} G_{JJ} & G_{JB} & G_{JT} \\ G_{BJ} & G_{BB} & G_{BT} \\ G_{TJ} & G_{TB} & G_{TT} \end{bmatrix} \cdot \begin{bmatrix} T_J \\ T_B \\ T_T \end{bmatrix} \quad (6)$$

where P designates heat currents, G the conductance values, T the temperatures, and the J,B,T subscripts refer to the junction, the bottom and the top, respectively. We intend to express the elements of the G conductance matrix with such measured values that we measure on the chip, while on the other ports only the terminations are varied.

In the first phase of the calculation let us consider only the junction/bottom two-port, the third port is assumed to be permanently short-circuited, that is thermally grounded. In this case the above equation reduces to a two-port one. This static two-port equation for the junction/bottom ports can be written as

$$\begin{bmatrix} P_J \\ P_B \end{bmatrix} = \begin{bmatrix} G_{JJ} & G_{JB} \\ G_{BJ} & G_{BB} \end{bmatrix} \cdot \begin{bmatrix} T_J \\ T_B \end{bmatrix} \quad (7)$$

Supposing the termination with $k \cdot R_{ps}$ thermal resistance on the port B the relationship between T_B and P_B can be expressed as

$$T_B = -k R_{ps} P_B \quad (8)$$

After some rearrangements of equations (7) and (8) we can express the value of the thermal conductance measured on the junction port, that is P_J/T_J for the case when the top is grounded and the bottom is terminated with a $k_n \cdot R_{ps}$ thermal resistance:

$$G_{BnT0} = G_{JJ} - \frac{G_{JB}^2}{G_{BB} + 1/k_n R_{ps}} \quad (9)$$

where k_n is the multiplier of the used polystyrene layer, given in Table 1. To obtain this equation $G_{JB}=G_{BJ}$ has been considered, assuming the reciprocity of the thermal network. G_{JJ} is equal to G_{B0T0} per definition. G_{BB} and G_{JB} can be determined if we have data for different k values. Using Eq. (9) for two different k_x values yields in

$$G_{BB} = \frac{(G_{JJ} - G_{BxT0})/k_x R_{ps} - (G_{JJ} - G_{ByT0})/k_y R_{ps}}{G_{BxT0} - G_{ByT0}} \quad (10)$$

This equation provides the value of G_{BB} . To determine the value of G_{JB} Eq. (9) has to be applied. With the data given in Table 2 we obtain the following conductance values:

$$G_{BB} = 0.87 \text{ W / K}, \quad G_{JB} = -0.795 \text{ W / K}.$$

For the third, "top" port the same procedure can be applied to calculate the G_{TT} and G_{JT} elements of the steady-state conductance matrix. Finally the G_{TB}

element can be determined using the fact that the steady-state conductance matrix is always indefinite, in other words its determinant is zero.

4.2. Identification of the dynamic model

To identify the time dependent components of the model the frequency domain appeared to be more convenient than the time domain since here the calculations may be accomplished by algebraic operations. For this reason first all the measured time responses (like the few ones shown in Fig.11) were transformed into the frequency domain. For this transformation a convolution-type algorithm was used [17] which is a built-in service of the software of the applied thermal transient tester [11]. The resulting complex loci are plotted in Fig. 12. These curves are the frequency dependent, complex port impedances at the port J. These impedance functions are distinguished according to the terminations of the B and T ports, as $z_{B0T0}(\omega)$ etc. The reciprocals of these functions, the $y_{B0T0}(\omega)=1/z_{B0T0}(\omega)$ admittance functions will be also used.

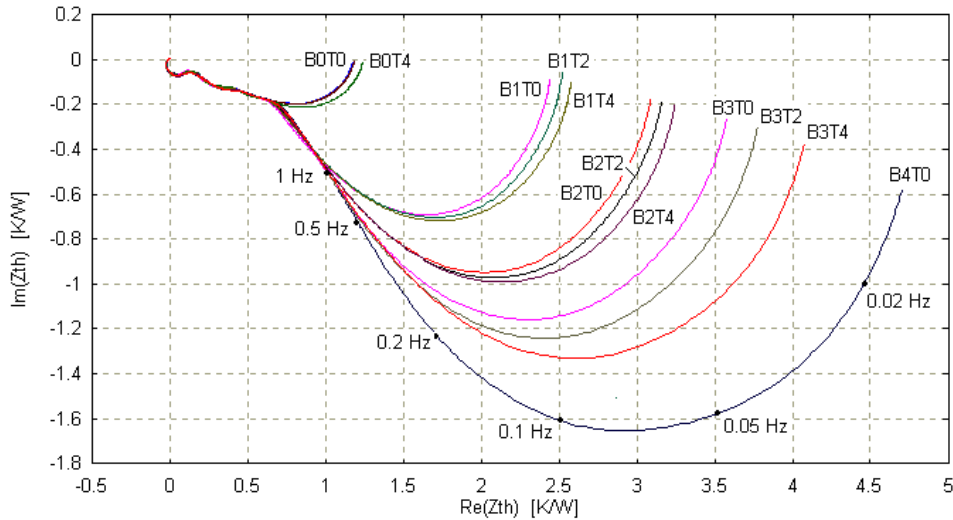


Fig.12. Thermal responses in the frequency domain (impedance loci)

A thermal three-port, considered at the J(junction), B(bottom) and T(top) ports, may be described in the frequency-domain - similarly to the steady state case - by a matrix description, The relationship between the alternating heat currents and the temperatures at the different terminations may be given in the frequency domain by the frequency dependent y admittance matrix as follows (like Eq.(2)):

$$\begin{bmatrix} p_J \\ p_B \\ p_T \end{bmatrix} = \begin{bmatrix} y_{JJ} & y_{JB} & y_{JT} \\ y_{BJ} & y_{BB} & y_{BT} \\ y_{TJ} & y_{TB} & y_{TT} \end{bmatrix} \cdot \begin{bmatrix} \tau_J \\ \tau_B \\ \tau_T \end{bmatrix} \quad (11)$$

To determine the elements of the frequency dependent admittance matrix we have to find first in general how they can be determined from measured results – preferably from results measured at the chip (junction) port, while on the other ports only the

terminations are different. In finding these elements we follow the same steps as in the steady state case. These elements will have to be modeled in the second step by a model network.

The elements of the admittance matrix may be determined in the following steps:

4.2.1. Determining y_{JJ}

If the termination is short-circuit on both the B and T ports then $\tau_B=\tau_T=0$. For this case the first row of Eq. (8) reduces to

$$p_J = y_{JJ} \tau_J \quad (12)$$

It is obvious that in this case y_{JJ} is equal to the port impedance, that is :

$$y_{JJ} = y_{B0T0}. \quad (13)$$

4.2.2. Determining y_{JB} and y_{BB}

In this case we apply the B1T0 and B4T0 boundary combinations. This means that port T remains short-circuited ($\tau_T=0$) and port B is terminated by the 1st and the 4th polystyrene layer, respectively. For the termination of the B port we can write

$$p_B = -\tau_B / kR_{ps} \quad (14)$$

By substituting this equation in Eq. (11), considering ($\tau_T=0$) yields in

$$y_{BnT0} = y_{JJ} - \frac{y_{JB}^2}{y_{BB} + 1/k_n R_{ps}} \quad (15)$$

where the $y_{JB}=y_{BJ}$ identity has been exploited again. Eq. (15) when applied for $n=1$ and $n=4$ provides a system of linear equations for the two unknowns of y_{BB} and y_{JB}^2 . From this system of equations y_{BB} can be expressed as follows:

$$y_{BB} = \frac{(y_{JJ} - y_{B1T0})/k_1 R_{ps} - (y_{JJ} - y_{B4T0})/k_4 R_{ps}}{y_{B1T0} - y_{B4T0}} \quad (16)$$

Knowing the value of y_{BB} , y_{JB} can be determined from Eq.(15) [16].

4.2.3. Determining y_{BT}

This admittance can be calculated from the measured one if finite termination is present on both the B and T ports. In terms of polystyrene layer numbers a y_{BnTm} admittance function has to be used, where $n, m > 0$. Taking into consideration these terminations the y_{BT} function can be determined from the equation of

$$\det \begin{vmatrix} y_{JJ} - y_{BnTm} & y_{JB} & y_{JT} \\ y_{BJ} & y_{BB} + 1/k_n R_{ps} & y_{BT} \\ y_{TJ} & y_{TB} & y_{TT} + 1/k_m R_{ps} \end{vmatrix} = 0 \quad (17)$$

During the practical calculations however we are facing characteristic difficulties. While the low frequency end of the impedance functions as e.g. y_{BB} can be easily calculated the high frequency end became ambiguous and finally suppressed by the measurement inaccuracies. The origin of this problem lies in the fact that in the denominator of Eq. (16) the difference of two measured port admittance values $y_{B1T0}-y_{B4T0}$ is calculated and the difference of these impedance functions vanishes at higher frequencies, above 0.5 Hz. This fact is very clearly shown in Fig. 12.

This observation is not surprising, knowing that the y_{BB} admittance is the input admittance of the B port, that we try to measure using the J port. By changing the termination on the B port this is possible for low frequencies. There is no way, however, to "see across" the multiport in order to sense the high frequency behavior of the B port, since the transfer path from the J port to the B port consists of sections having much lower cutoff frequencies.

The only way to avoid this problem is to finish the calculation of the complex loci when the denominator of Eq. (16) falls under a certain limit.

The admittance curves shown in Fig. 13 have been calculated this way.

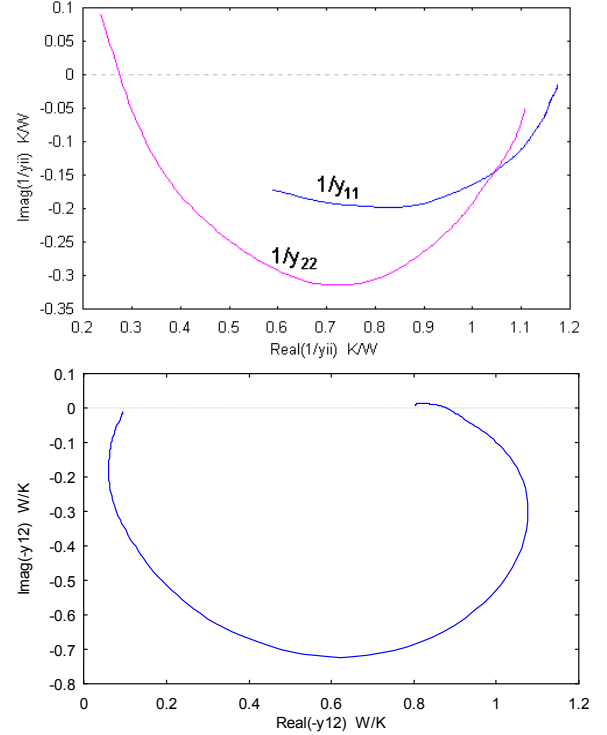


Fig.13. Complex loci of the identified admittance functions. The frequency range is 0.01 Hz - 15 Hz for y_{11} and y_{12} , 0.01 Hz - 1 Hz for y_{22} .

3.2.4. Generating an electrical equivalent circuit

The next step of the identification is to model each admittance function by an RC network. First the admittance/impedance functions have to be approximated by a pole and zero arrangement, then the model network has to be assembled [17,18]. The ladder type networks suggested by the first part of the paper are suitable. The calculation of their elements based on the pole-zero data is now already an easy task.

The complete multi-port package model can be constructed in the generic form presented in Fig.6. This way of the multi-port thermal model construction has been outlined formerly by the authors, in the context of electro-thermal simulation [19,20]. In this approach all the elements of the y matrix are modeled individually by distinct RC one- or two-ports and these sub-networks are coupled by an array of linear controlled sources.

Note, that the y_{JJ} admittance does not suffer from the limitations caused by the ambiguities at higher frequencies since this admittance is measured directly on the junction-port of the package. This means that the y_{JJ} admittance can be modeled in more details, following the same methodology as the one elaborated for the one-port modeling [18]. Since it is always the chip itself where the fast transients occur the high frequency limitations on the other ports have no practical effects on the accuracy of the

entire model.

In order to verify the presented way of model construction a model has been generated, based on the admittance loci of Fig. 13. In this simple model the "top" node has been considered short-circuited. The y_{JJ} admittance has been modeled in details by using a ladder model. The R and C values of the ladder were calculated by the algorithm described in [18]. For the y_{BB} admittance a two-elements model was used while the $y_{JB} = y_{BJ}$ admittances were modeled in a rough approximation by single conductances. The model was evaluated by using a general-purpose network simulation program. The results are presented in Fig. 14. for three different terminations of the "bottom" side. In order to make the comparison easy the measured curves are plotted as well. It can be concluded that the match of the responses is generally good. In the time range of 0.1-1s, however, perceptible differences can be observed. In our opinion a more detailed modeling of the y_{JB} and y_{BB} admittances could reduce this inaccuracy.

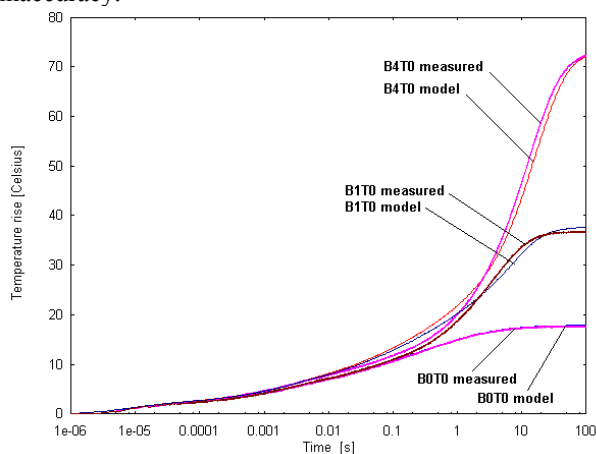


Fig. 14. Comparison of the measured and model responses

5. Conclusions

A generic form of multi-port thermal package models is presented, which seems to be well suited for the calculation of dynamic thermal problems.

The parameters may be obtained from simulations or from measurements. We tried to develop a method for multi-port, dynamic package model generation, where the model parameters are generated automatically from thermal transient measurements taken via the chip only.

Our investigations have proven the feasibility of measuring chip-external parameters from the chip, but the evaluation requires highly accurate measurements. By using simulation results of a detailed package model much more accurate responses can be obtained and the model identification may be easier – if we know all the exact material parameter values, which is frequently not the case.

An important conclusion of our investigations is that measuring from the chip side only the parts responsible for the low frequency behavior can be determined for the far side of the model. This is however not a serious problem, since we are always interested in the accurate modeling on the chip side.

One of the biggest challenges in our measurements was to assure exact thermal resistance values for the terminations. The repeated mounting - dismounting of the DCP measurement set-up was rather inconvenient, demonstrating the need for an externally controllable thermal resistance that was investigated in [21].

6. Acknowledgements

This work was partially supported by the PROFIT IST-1999-12529 Project of the EU, and by the T025820 and T025817 OTKA, and the FKFP 0385/1997 projects of the Hungarian Government. The extensive help of S.Török, E.Kollár and L.Pohl in doing the measurements is acknowledged.

7. References

- [1] **B.S. Siegel**: "Measuring thermal resistance is the key to a cool semiconductor", *Electronics*, V.51, pp. 121-126 (1978)
- [2] **V. Székely and Tran Van Bien**: "Fine structure of heat flow path in semiconductor devices: a measurement and identification method", *Solid-State Electronics*, V.31, pp. 1363-1368 (1988)
- [3] **W. Sofia**: "Analysis of thermal transient data with synthesized dynamic models for semi-conductor devices", *IEEE Trans. on Comp. Pack. & Manuf.* V.18, No.1. pp. 39-47 (1995)
- [4] **G. Oliveti, A. Piccirillo and P.E. Bagnoli**: "Analysis of laser diode thermal properties with spatial resolution by means of the TRAIT method", *Microelectronics Journal*, V.28, No.3. pp.293-300 (1997)
- [5] **A. Bar-Cohen and W.B. Krueger**: "Thermal characterization of chip packages – evolutionary development of compact models", *SEMI-THERM'97*, 28-30 January, 1997, Austin, USA, Proceedings pp. 180-197
- [6] **C.J.M. Lasance, D. den Hertog, P. Stehouwer**: "Creation and evaluation of compact models for thermal characterisation using dedicated optimisation software", *SEMI-THERM'99*, 9-11 March, 1998, San Diego, USA, Proceedings pp.189-200
- [7] **H. Pape, G. Noebauer**: "Generation and verification of boundary independent compact thermal models for active components according to the DELPHI/SEED methods", *SEMI-THERM'99*, 9-11 March, 1998, San Diego, USA, Proceedings pp.201-211
- [8] **F. Christiaens, B. Vandeveld, E. Beyne, R. Mertens, J. Berghmans**: "A Generic methodology for Deriving Compact Dynamic Thermal Models, Applied to the PSGA package" *IEEE Trans. On Components, Packaging and Manufacturing Technology, Part A* Vol 21, No.4 Dec.1998 pp 565-576
- [9] **V. Székely, M. Rencz, B. Courtois**: "Application results of a new thermal benchmark chip", *SEMI-THERM'98*, 10-12 March, 1998, San Diego, USA, Proceedings pp.3-39
- [10] **Wai-Kai Chen** (ed. in chief): *The Circuits and Filters Handbook*, CRC Press & IEEE Press, Boca Raton 1995,

- [11] <http://www.micred.com/index1.htm>
- [12] **V.Székely et al.**: Transient thermal measurements for dynamic package modeling: new approaches, 5th THERMINIC Workshop, 3-6 Oct. 1999, Rome, pp 7-11
- [13] **S. Röss, E. Kollár** : “Comparison of various thermal transient measurement methods on a benchmark package”, Proceedings of the 6th THERMINIC Workshop, Budapest, 24-27 Sept. 2000 , pp 120-123
- [14] **H.I Rosten et al.**: Final Report to SEMITHERM XIII on the Europea –Funded Project DELPHI – The Development of Libraries and Physical Models for an Integrated Design Environment, SEMITHERM XIII, Austin, TX, USA, Jan. 28-30, 1997. Proceedings, pp 73-91
- [15] **J. E. Sergent, Al Krum**: Thermal Management Handbook, McGraw-Hill, New York, 1998
- [16] **M.Rencz, V.Székely, E.Kollár**: “Measuring dynamic thermal multiport parameters of IC packages”, Proceedings of the 6th THERMINIC Workshop, Budapest, 24-27 Sept. 2000 , pp 244-250
- [17] **V. Székely**: Convolution calculus in the network theory and identification, ECCTD 1997, Budapest 30 August - 3 Sept. 1997, pp. 49-56.
- [18] **V. Székely**: A New Evaluation Method of Thermal Transient Measurement Results. Special Issue of the THERMINIC Workshop, *Microelectronics Journal*, Vol. 28, No. 3, pp. 277-292, (1997)
- [19] **M. Rencz, V. Székely, A. Páhi, A. Poppe**: An alternative method for electro-thermal circuit simulation, Southwest Symposium on Mixed-signal design, April 11-13 1999, Tucson, Arizona, USA, pp. 117-122
- [20] **V. Székely, M. Rencz, B. Courtois**: A step forward in the transient thermal characterization of chips and packages. *Microelectronics Reliability*, January 1999, Vol. 39, Nr. 1, pp. 89-96
- [21] **V. Székely, A. Nagy, S. Török, G. Hajas, M. Rencz**: Heat sinks with controlled thermal resistance: an experiment. Proceedings of the Therminic Workshop'99, 3-6. October, Rome, Italy, pp. 249-251