Thermal Qualification of 3D Stacked Die Packages

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Abstract

In this paper measurement experiments prove that the structure function evaluation of the thermal transient testing is capable to locate die attach failure(s), even in case of stacked die packages. Both the strength and the location of the die attach failure may be determined with the methodology of a fast thermal transient measurement and the subsequent computer evaluation. The paper summarizes shortly the theoretical background of the method, and presents the use of the methodology with several measured examples. With the help of the presented correction procedure even the accurate values of the thermal layer parameters, such as thermal resistances or capacitances may be determined with the discussed thermal qualification methodology.

1. Identifying the partial thermal resistances and capacitances in stacked die packages with the help of the structure functions

The reliability of packaged electronics strongly depends on the quality of the die attachment. Any void in it or a small delamination may cause instant temperature increase in the die, leading sooner or later to failure in the operation. Since die attach problems are built in time bombs, they have to be eliminated by any means. They usually can not be detected by the electronic test, only in special, very bad cases. They can be detected by steady state thermal measurements, but these measurements can only indicate but not locate the actual problem. In case of 3D stacked die structures, that will dominate the packages in the near future the die attach quality control problem is multiplied: the structure contains as many die attach layers as the number of dies. These are very difficult to test, resulting in pronounced reliability concerns.

It has been presented already earlier that the structure functions [1] are appropriate to locate die attach failures in single die packages [2]. In the paper of [3] we have presented simulation results that predicted that with the help of the structure functions we can determine the location of die attach failures in case of stacked die packages.

The structure functions provide a map of the cumulative thermal capacitances with respect to the thermal resistances measured from the location of the heating to the ambient. In the derivative of this function, in the so called differential structure function the square of the heat current-flow cross section area is represented as a function of the cumulative resistance. In both these functions the local peaks and valleys indicate reaching new materials in the heat flow path, and their distance on the horizontal axis gives the partial thermal resistances between them. More precisely, the peaks point usually to the middle of any new region where both the areas, perpendicular to the heat flow and the material are uniform. After identifying the peaks that refer to the chip and the chip carrier their distance on the horizontal axis can be read from the diagram. This value gives the die attach thermal resistance.

The method can be used for detecting die attach failures as follows.

(1) The structure function of a good sample has to be created. This can be obtained by mathematical transformation [1] of the measured or simulated thermal transient curves.

(2) The structure function of the sample package that we wish to evaluate has to be created from the thermal transient curves, measured on the devices under test, and with the same mathematical transformations.

(3) The structure function of the known good device has to be compared to the structure function of the device under test. The shift in the appropriate points in the structure functions gives the increased thermal resistance of the layer in question.

The special advantage of the method is, that it normally does not require any additional elements on any of the stacked dies, as the substrate diode of any silicon die can be used both as heater and temperature sensor for the thermal transient testing of the structure. In the presented examples we used mostly thermal test dies, but this is of course not a prerequisite of the application of the method. Using test dies helped however in the cross-checking of the measured results, and these cross-checking calculations are presented in the paper.

In the next section first we present how the method works in practice. We demonstrate with measurements carried out on various packages, containing 3D stacked dies how to recognise and locate the differect die attach problems from the different visualizations of the structure functions, or other curves that can be constructed from the evaluation of the thermal transient curves. At the end of the paper we present a correction methodology, which enhances the accuracy of the method such, that the die attach thermal

resistance values can be also determined with good accuracy from the structure functions.

2. Verification of the methodology by measurements

In the first series of measurements we measured packages that contained stacked thermal test dies [4] in a pyramidal structure packaged in LQFP144 packages. [5] The cross section of these packages is presented in Figure 1. The measurements were done by T3ster [6].

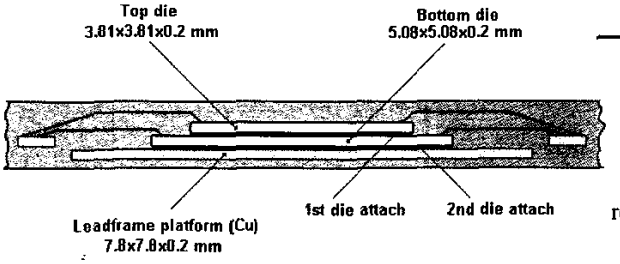

Figure 1: Cross section of the measured packages

In the first experiment the top die was used as heater and temperature sensor. The structure function constructed from the measured heating curve is shown in

Figure 2.

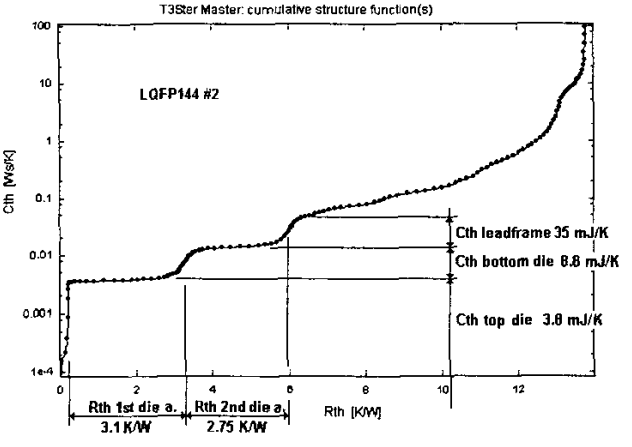

Figure 2: The obtained structure function

The data we can read from this figure are in good agreement with the hand-calculated values, we can verify this as follows. For the upper chip: calculating the volume with 150×150 mils = 3.81×3.81mm^2 area and 0.2 mm thickness, and considering 1.66×10^6 Ws/m^{3}K volumetric heat capacity for the Si, the obtained Cth value is 4.8×10^{-3} Ws/K. For the bottom chip: calculating with 200×200 mils = 5.08×5.08 mm^2 and considering 0.2mm thickness value, the obtained Cth value is 8.57×10^{-3} Ws/K. For the Cu platform: calculating the volume with 7.8×7.8 mm area and 0.2 mm thickness, and considering 3.44×10^6 Ws/m^{3}K volumetric heat capacity for the Cu, the obtained Cth value is 40.6 Ws/K. For the sake of comparison refer to Table 1.

	Top die	Bottom die	leadfra me
Hand calculated	4.8	8.57	40.6
Read from the structure function	3.8	8.8	35

Table 1: Comparison of the hand calculated and measured Cth values in 10-3 Ws/K

As it is readable from the table, the values agree reasonably.

In this case the thermal resistance obtained for the 1st die attach may be verified by a static measurement as well. Since both dies are thermal test dies the temperature difference between them can be easily measured. The heating curves of the two dies are presented in Figure 3.

The steady state temperature difference of the two dies can be read on the right had side of the figure, this is 1.61 °C. The heat flow between them is more or less the whole dissipation, neglecting the small heat flow exiting on the package top, consequently Rth 1st die attach = 1.61/0.397 = 4.05 °C/W. This value is close to the 3.1 °C/W value read from the structure function of

Figure 2, but the difference is not negligible.

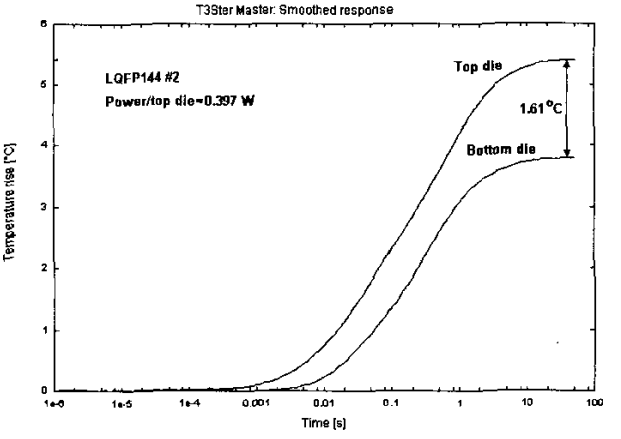

Figure 3: The measured thermal transients on the two packages

An explanation can be given with the help of the rough 3D compact model of the structure presented in Figure 4.

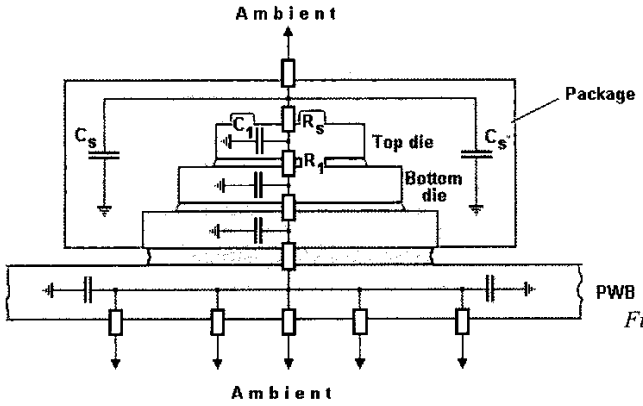

Figure 4: Dynamic compact thermal model of the packaged stacked die structure

The smallest (first) characteristic time constant of the vertical structure represented by the structure function is given by the $\tau=R_1C_1$ value, where C_1 is the thermal capacitance of the top die, and R_1 is the thermal resistance of the first die attach under it. This time constant provides the data for the first step of the structure function of Figure 2.

The R_S thermal resistance of the mould together with the thermal resistance representing the heat flow upwards and the C_S thermal capacitance of the package are connected parallel to the chain of the main heat flow path. The R_SC_S branch is active only dynamically, since the C_S capacitance acts as an open circuit in steady state. During the switching, that is, in the first seconds of the transient measurements this C_S capacitance behaves as a short circuit, connecting the shunt resistance of the mould parallel to the RC chain of the main heat flow path. This means that systematically we have to expect smaller measured R_{th} values for the first elements of the chain than the real values. Knowing however the parameters of the shunt circuitry we can correct the structure function as it is presented in [7].

The measurements on all the samples provided the same data, so we could not detect erroneous packages among the samples examined.

In the second series of measurements presented here similar experiments were carried out on several samples of a 44lead QFN (Quad Flat No-lead) package, denoted as EM2. In this case however some of the samples have earlier been subjected to accelerated moisture and temperature shock testing to induce different extent of interfacial integrity.

The cross section of this package is presented in Figure 5.

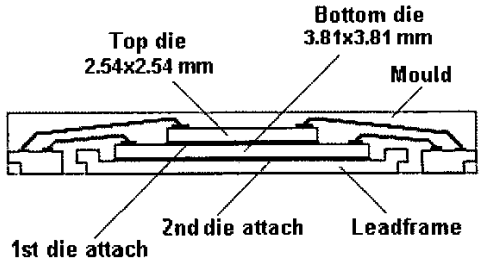

Figure 5 Cross section of the 44L QFN packages, denoted as EM2 series

This package contained also thermal test dies, and the top die was used to heat and measure the temperature in the middle of the structure. Two samples were examined, denoted by EM2 and EM2-2.

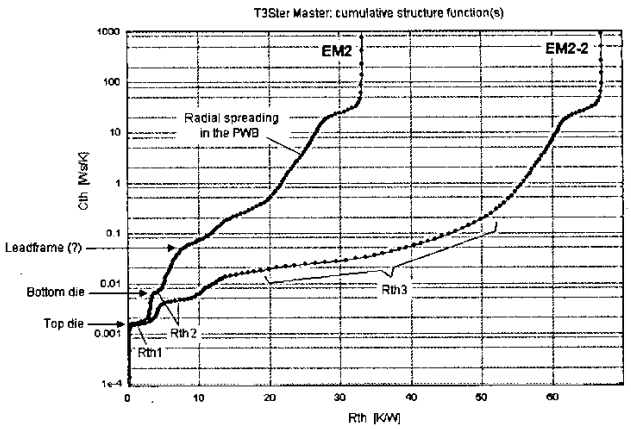

Figure 6 The cumulative structure functions of the two 44L QFN packages

The top die thermal capacitance of Figure 6 refers to a 1.05 mm^3 volume of silicon. The volume of the top die calculated from Figure 5 is 2.54×2.54×0.2 = 1.3 mm3. "Bottom die" in Figure 6 shows the thermal capacitance value of the bottom die. From this value the calculated volume of the bottom die is 3 mm3, while 3.81×3.81×0.2=2.9 mm3 volume is expected from Figure 5. This difference is fairly small (~3%). In case of the package denoted as EM2-2 this thermal capacitance value is smaller, which is probably originating from the detected anomalies, most probably delamination in the further regions of the heat flow path.

The almost horizontal section under the top die denoted by Rth1 is the thermal resistance of the die attach under the top die. It is slightly increased for the sample denoted by EM2-2, the values are: ~2.7 K/W and ~3.8 K/W, suggesting a small delamination in the package EM2-2 in the upper die attach layer.

The second almost horizontal section denoted as Rth2 is the thermal resistance of the die attach under the bottom die.

This is strongly different at the two samples: EM2 ~1.6 K/W, EM2-2 ~5 K/W, and before reaching the thermal capacitance of the lead-frame we can identify a further large almost horizontal part demonstrating a largely increased thermal resistance, shown by Rth3 in Figure 6. This resistance can be even better seen from a figure where the structure functions of the two samples are drawn up in one figure, and the curve of the known good one is copied and shifted to demonstrate the fit on the right hand side, see Figure 7. The section where the curve denoted as EM2-2 travels alone shows the increased thermal resistance on the EM2-2 sample. Since this section of the curve is running entirely under the capacitance value attributed to the lead-frame this curve indicates the presence of an increased thermal resistance between the bottom die and the lead-frame.

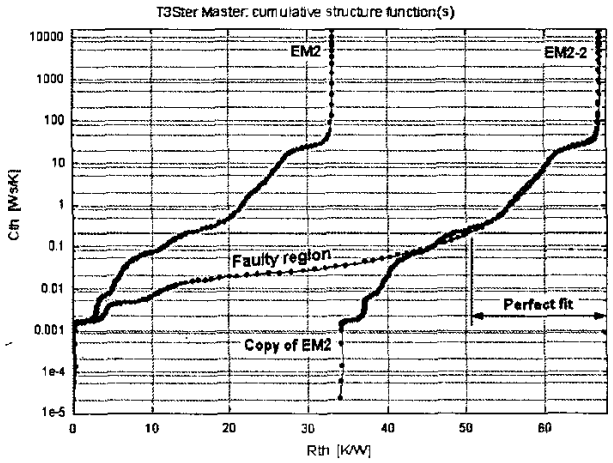

Figure 7 Cumulative structure functions of the two samples, a copy of the EM2 curve is shifted to match at the right end.

We can state from this large shift that there is probably a strong delamination at this sample between the lead-frame and the bottom die. This statement has been verified by C-mode Scanning Acoustic Microscope inspections, revealing in fact delamination of the bottom die.

With the help of these test dies in the packages the coupling between the dies can also be examined. In the figures below the frequency plots of the chip temperatures are presented for the good EM2 and the faulty EM2-2 packages, see Figure 8 and Figure 9, respectively.

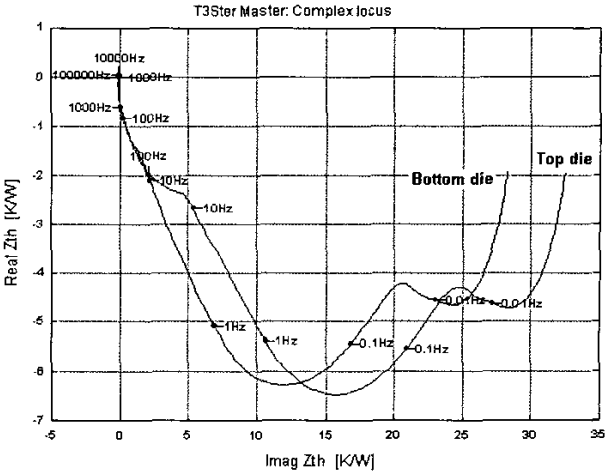

Figure 8: Frequency plot of the complex thermal impedances of the two chips when the EM2 package is measured on a JEDEC standard board in still air chamber, the top die is excited.

In both measurements the top dies were heated and the temperatures were observed in both the top and the bottom dies. As it is shown in these figures the thermal resistance values in Figure 9 are much higher than in Figure 8, and the coupling between the two dies is much weaker. These figures suggest also that the EM2-2 chip was the one subjected to MSL-1 pre-conditioning[1], resulting in the degradation of the interface integrity.

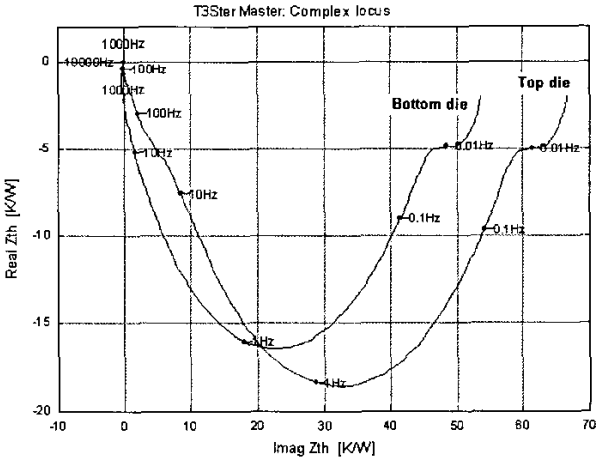

Figure 9: Frequency plot of the complex thermal impedances when the EM2_2 package is measured on JEDEC standard board in still air chamber, the top die is excited.

[1] MSL stands for Moisture Sensitivity Level

3. Correction of the results with the consideration of the parallel heat flow path

In case of stacked die packages, especially if we wish to determine the exact thermal conductivity values of the layers we have to consider also the effect of the parallel heat flow path, which modifies our measured results. The effect of the parallel heat flow path may be considered and the structure function can be corrected as it was presented in [8]. For the correction we have to find first the path where the heat is escaping from the die, parallel to the die - cold plate path, from which we calculate the thermal parameters. Studying the structure of the examined package on the slightly distorted model of Figure 10 (the distortion in the aspect ratio is 2.5:1) we see that the most important parallel path is the one, upwards from the top die. We can determine the structure function of this region by inserting a very thin (virtual) insulator layer under the location of the dissipation, in order to force all the heat to move upwards from the top die, and check the thermal transients of this artificial heat flow path by simulation. It can be proven by simulation that subtracting the structure function of this "error" region from the structure function of the measured structure an about 30% correction can be obtained in the thermal resistance values. The correction has much less influence on the thermal capacitance values.

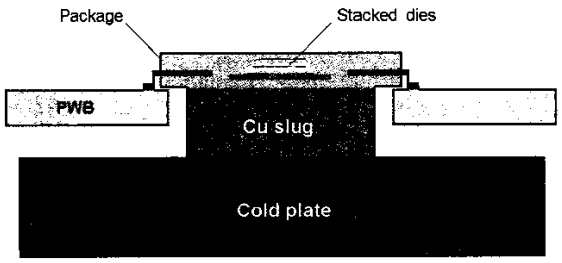

Figure 10 The simulation model of the package of Figure 1

Figure 11 shows the corrected structure function of the stacked die structure of Figure 1. On this figure A denotes the structure function that can be calculated from the measured results, **B** denotes the corrected structure function. As it can be read from this figure the correction appears first in the value of the thermal resistance of the first die attach layer, and practically the same shift is characteristic for the rest of the structure function. The thermal capacitance values are practically not influenced by this correction.

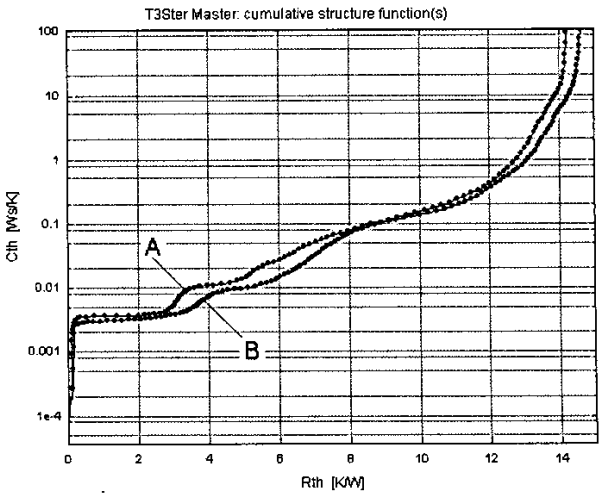

Figure 11 Correction of the results with the parallel heat flow path

The correction procedure raises a lot of further question. We wish to answer also these in the final version of the paper.

4. Conclusions

With the presented measurement experiments we have demonstrated the feasibility of locating die attach problems in stacked die structures. In the proposed methodology first the thermal transient response of the structure has to be obtained from measurement, and from this the structure functions have to be calculated. Comparing the structure functions of a measured sample with the appropriate structure functions of a known good stacked structure, which can be obtained e.g. from the simulation of the structure, the differences can be easily observed. From the location of the shift in the structure function of the device under test , in case of structures with die attach problems, the location of the die attach problem can be determined.

The method works well both in the case of stacked dies of the same size, and in the case of pyramidal stacked die structures. The resolution of the method will be further investigated with different die sizes and layer numbers, but from the simulation experiments up to now it can be expected that the method is well applicable for structures up to 3-4 layers of stacked dies.

A special advantage of the methodology is that for the presented technology test dies are actually not needed, any working die can be used both as heater and temperature sensor in our methodology. For measuring the structure function we even do not need any extra elements on the dies if the substrate diodes of the individual dies are not connected electronically, since for temperature sensing the substrate diode of the top die may be conveniently used. If for some reason the substrate diodes of the dies have to be

connected electrically, other dedicated elements have to be selected on the dies for temperature sensing.

On the other hand, switching on either the whole dissipation on the top die, or just one dissipating element, may provide the constant source of heat during the time of the transient measurement. This means that obtaining the necessary transient curves is feasible normally without any special built in elements or test structures in any circuit.

This way we may conclude that with the presented method the fast diagnosis of the die-attach problems of stacked dies is possible, and the method does not require any additional circuit elements in any of the stacked dies.

Acknowledgments

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