



24-26 September 2008, Rome, Italy

Design of a static TIM tester

V.Székely, G.Somlay, P.G.Szabó, M.Rencz
Budapest University of Technology & Economics
Department of Electron Devices
szekely|somlay|szabop|rencz@eet.bme.hu

Abstract- Nowadays the quality of thermal interface materials (TIM) has a growing importance as the increasing dissipation level of ICs requires more and more sophisticated solutions to reduce the R_{th} along the heat-flow path. The recent approach of TIM manufacturers is to use nanoparticles as fillings in TIM materials, in order to enhance considerably the TIM thermal conductivity. On the other hand this solution raises difficulties in the characterization of these materials. Namely, the resolution of the conventional methods is not high enough to measure resistance values as low as 0.01-0.05 Kcm²/W. This is the reason why we developed static TIM tester equipment using some new concepts. The main idea behind our design is to use the capabilities of microelectronics in order to make small sized sensors both for temperature and heat flux sensing. This way it is possible to place these sensors in the closest proximity of the measured sample. The status of this work is presented in the paper.

I. INTRODUCTION

For the measurement and characterization of the TIMs properties many methods have been designed, however most of them are based on the ASTM standard D-4570. This test procedure is a standard method to measure thermal resistance and bulk conductivity for TIMs such as greases, pads, tapes and phase change materials. The inspected TIM sample is placed between a hot and a cold meter bar and a constant heat flux is applied. The ASTM test defines thermal resistance per unit area (θ) to include the thermal resistance of the material ($\theta_{material}$) plus the interfacial contact resistance of the TIM to the substrates ($\theta_{interface}$). The heat resistance of the tested material is calculated from the known heat flux forced through the tester and from the measured heat drop.

The ASTM standard also prescribes that the temperature measurements should be done at a clamping force of 3 MPa to reduce the heat resistance between the calorimeters or heat flux meters and the specimen.

This standard is only valid under the following assumptions:

- One dimensional heat flow
- Thickness does not change during measurement
- Contact resistance does not depend on thickness

The most severe shortcoming of the ASTM method is its use of higher pressure than used in real applications [1]. The high pressure reduces the contact resistance between the specimen and the meter bars. In cases of greases and phase change materials the high pressure will result a lower gap, therefore the total θ_{total} will be lower than in an actual application.

Tester based on this standard was used in the measurement of CNT (carbon nanotube) array based TIM for the thermal management of microelectronic packages and high brightness light emitting diode (HB-LED) packages [2].

To obtain a profile of the temperatures across the interface a thermal test vehicle has been developed and presented in [3]. This information provides insight into uniformity of the thermal resistance and provides information about the performance of TIMs over their life cycles.

At Sun Microsystems, Inc. the ASTM standard tester has been modified in both the hardware and methodology to allow measurement of high-performance TIMs under conditions that more closely resemble the use-condition in application [4].

Due to the high (10-20%) reproducibility error of the standard a different method has been presented in [5]. The *Interface Thermal Resistance Tester (IRT)* consists of two silver cylinders between which the sample is clamped. The temperature of the lower block can be changed very fast with a jet impingement technique using two water baths. The temperature response of the upper block is a measure for the interface thermal resistance.

The resolution and the reproducibility of the conventional methods is not high enough to measure thermal resistance values as low as 0.01-0.05 Kcm²/W. This is the reason why we decided to develop static TIM tester equipment using some new concepts.

The main idea behind our design is to use the capabilities of microelectronics in order to make small sized sensors both for temperature and heat flux sensing [6]. This way it is possible to place these sensors in the closest proximity of the measured sample. Further new idea is to build a symmetrical structure with reversible direction of the heat flow, as certain inaccuracies of the measurement (as offset errors of the sensors) can be dropped out by making measurements in both direction of heat flow.

The principal parts of the measurement arrangement are shown in Fig.1. The heat flow is driven by two, symmetrically positioned Peltier cells. Both the heat flux and the temperature drop are measured by the two silicon dices constituting the grip area of the mount.

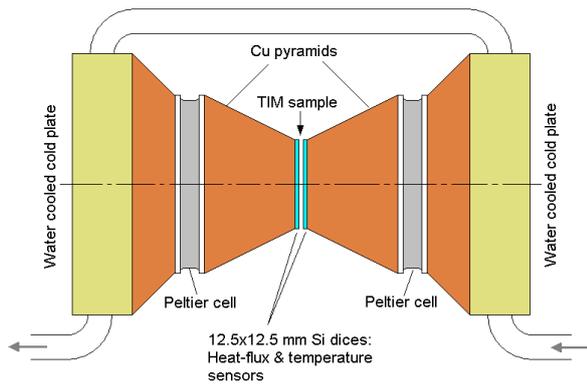


Fig. 1. The basic parts of the measurement arrangement

II. MECHANICAL DESIGN

The mechanical design of the assembly is shown in Fig. 2. (The arrangement is rotated by 90° with respect to Fig. 1.) **1** are the water-cooled cold plates, **2** are the Peltier cells. **3** are the Cu pyramids (one is rotated by 90 degree in order to make easier the contacting of the Si measurement dices (not shown in Fig. 2)). The lower mount is fixed to the base plate of the assembly while the upper one is moving in the vertical direction. The parallelism of the two grips can be adjusted by **3** screws (the related parts are **4** and **5** in Fig. 2). The height of the whole assembly is 150 mm.

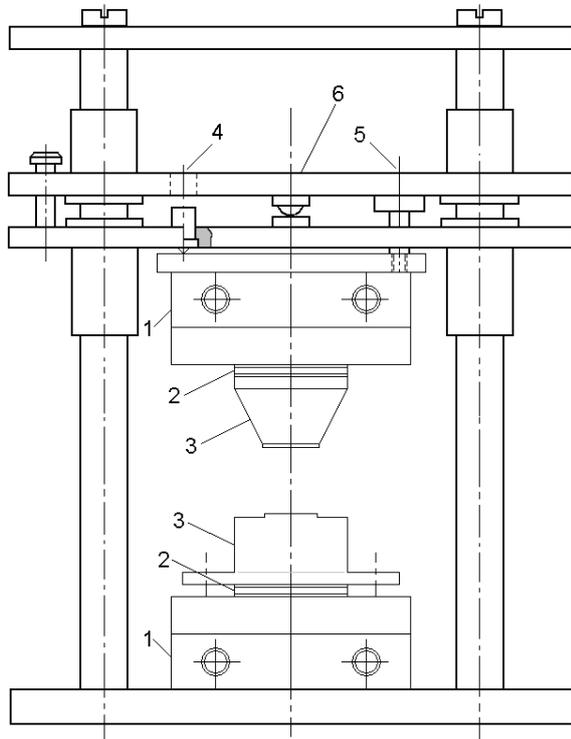


Fig. 2. The mechanical arrangement

In the present version the pressure is set by appropriate weights posed onto the plate **6**. In the further development a pneumatic pressure control is planned.

Photograph of the assembly is shown in Fig. 3.

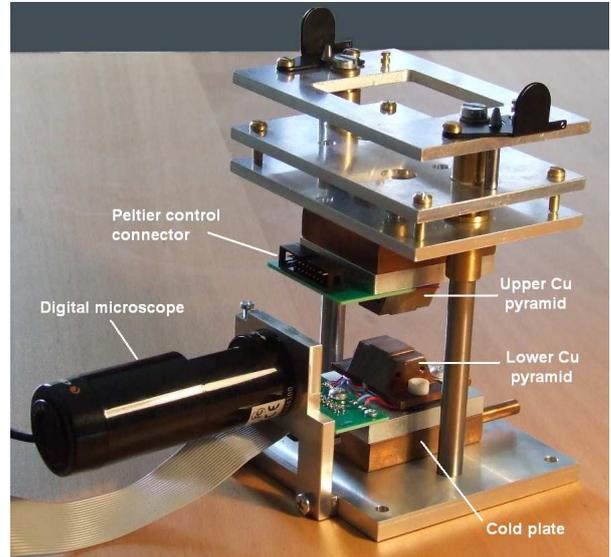


Fig.3. Photograph of the mechanical design

The region of the TIM sample and the upper/lower sensor chips is observed by a digital microscope. The same device is used to measure the thickness of the sample. The actual resolution is about 15µm/pixel. This parameter will be enhanced by using a more appropriate optics. A sample image of the microscope is shown in Fig.4.

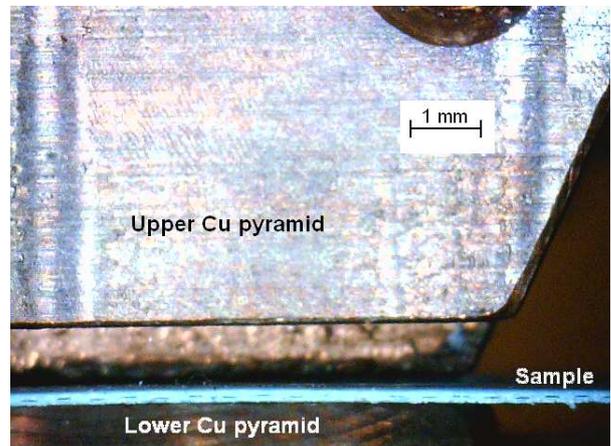


Fig.4. Image of the microscope observing the two grips of the sample holder (without the sensor chips). The thickness of the TIM foil (bright strip) is 250 µm.

III. DESIGN OF THE ELECTRONICS

The block diagram of the electronics is shown in Fig. 5. The two Peltier cells are controlled by the two identical

Peltier control units (PCUs). The thermal states of the Peltier cells are sensed by two temperature sensors ($TU1$, $TU2$ and $TL1$, $TL2$, respectively). Appropriate control of the Peltier currents IPU , IPL permits us to set different heat flux and temperature values on the sample under test.

The two silicon sensor chips lying on the two sides of the sample provides us with a voltage proportional to the heat flux (HFU , HFL) and with a voltage proportional to the temperature (TCU , TCL). These voltages are amplified and digitized by the two measurement units (MU1 and MU2).

The effective heat flux can be calculated as the mean value of HFU and HFL

$$HF = \frac{HFU + HFL}{2} \quad (1)$$

The thermal resistance of the sample is given by

$$R_{th} = \frac{TCU - TCL}{HF} \quad (2)$$

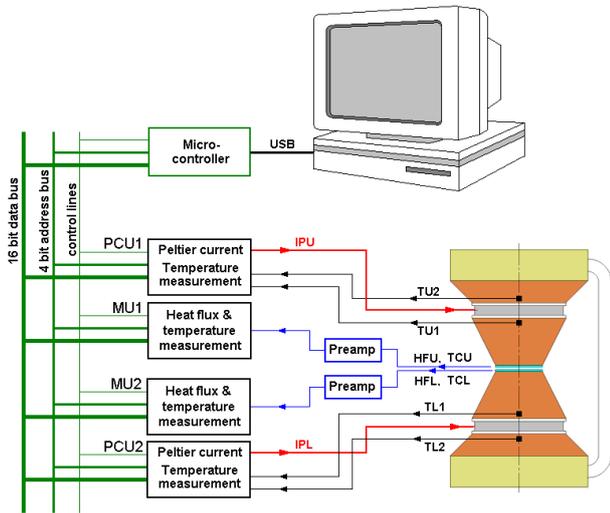


Fig. 5. Block diagram of the electronics. (PCU = Peltier control unit, MU = measurement unit).

In order to reduce the problems related to noise and disturbances the preamplifier stages of the measurement units will be placed in the closest proximity of the measurement chips. The photograph of a preamplifier unit is shown in Fig. 6.

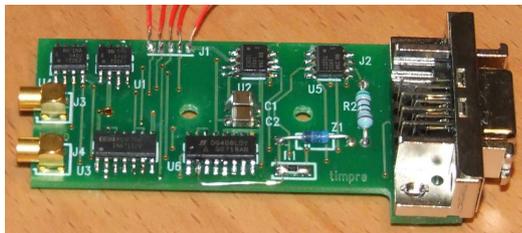


Fig.6. Preamplifier unit

The chip contains two Al-Si-Al gradient type heat flux sensors [7]. Both sides of the silicon dice are metalized, forming two Al-Si thermocouples which are serially connected but in counter direction. This means that the output voltage is proportional with the temperature difference between the two sides of the chip. This temperature difference is on the other hand proportional with the heat flux:

$$V_{out} = S(T_A - T_B) = SR_{thc}P \quad (3)$$

where S is the Al/Si Seebeck constant, T_A and T_B are the temperatures of the two sides; R_{thc} is the thermal resistance of the chip and P is the heat flux streaming through the chip.

The same sensor structures are suitable for temperature measurement as well, using the thermoresistance principle. The R_{el} electrical resistance of the sensor is temperature dependent, and may be considered with the following linear relationship:

$$R_{el} = R_{el0}(1 + \alpha_{el}(T - T_0)) \quad (4)$$

The α_{el} temperature coefficient is about 0.5-0.7 %/°C for medium doped p-Si that we use in our sensor.

The simplest layout of the chips that is mounted to the grip area is shown in Fig. 7. The two sensing areas cover 1 cm². Dividing the area into two halves was a need required both by the evaluation electronics and the control of parallelism. For measuring the electrical resistance the 4-wires arrangement is used in the chip.

The sensitivity of the chip is about 40 μ Vcm²/W in heat-flow sensor mode. In the temperature sensor mode we exploit the above mentioned temperature dependence of the sensor resistance.

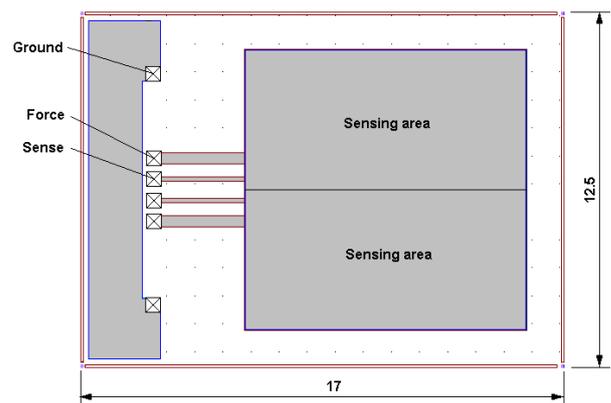


Fig. 7. Layout of the sensor chip

Some further chip versions like chip with more partitioning, chips with sensor structures for TIM thickness measurement, etc. are currently in the design phase.

A microphotograph of the chip is shown in Fig. 8. The chip is bounded to a very small printed wire plate, which in turn is connected to the preamplifier.

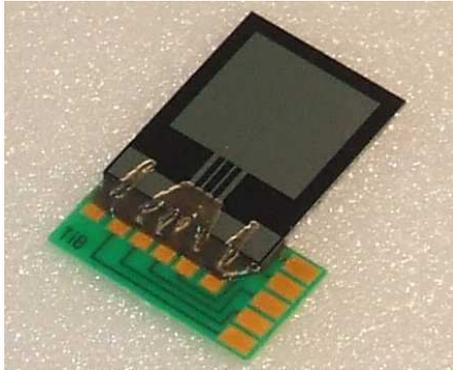


Fig. 8. The sensor chip

V. RESOLUTION, ACCURACY, CALIBRATION

The theoretical limit of the resolution of heat flux measurement is the LSB value determined by the amplifiers and the A/D converter. This LSB value is 4 mW. This very good value will obviously be reduced by the electronic noise. The measurements show that this noise remains below 2 LSB that means 8 mW. The resolution of temperature measurement is $LSB \approx 0.05^\circ\text{C}$. A dedicated circuit measures the temperature *difference* between the two chips. For this latter $LSB \approx 0.005^\circ\text{C}$. Since the maximum heat flux is about 40 W the expected resolution is $\sim 0.25\%$ for a sample with $R_{th} = 0.05\text{ K/W}$ and $\sim 1.2\%$ for 0.01 K/W.

In order to reach the suitable accuracy, the following components of the arrangement have to be calibrated:

- The thermoresistance of the sensor chips
- The sensitivity of the heat flux sensor
- Measurement of the sample thickness

In addition to these the parameters of the Peltier cells have to be determined/measured as well. These data are needed however for the control algorithm of the heat flow and hold little importance from the point of view of TIM resistance measurement accuracy.

The thermoresistances can be calibrated in the usual way, using a commercial thermostat. Since only the temperature difference appears in Eq. (2) there is no need to be very accurate in the absolute temperature but in the slope of the $R_e(T)$ diagram.

For the heat flux sensor an in-situ procedure is planned. A dissipator element (e.g. a transistor) will be placed between the grips of the sample holder. The injected heat flux can be calculated by using the drive voltage and current data. An obvious source of inaccuracy is that a small amount of heat leaves through the air to the ambience, instead of flowing through the sensor chip. In order to reduce this error an

active correction procedure can be used (besides good thermal isolation). With the help of the Peltier cells the structure can be cooled down until the dissipator reaches the ambient temperature. Without temperature difference the undesirable heat flow will be reduced significantly.

The partitioned heat flow sensor (see Fig. 7) provides an indirect way to observe and correct parallelism. The two chips are rotated each to other by 90° , as shown in Fig. 9. If the two chips are in perfectly parallel position¹ both the upper and the lower heat flow sensor pairs provide equal output signal. Unequal signals from the upper chip indicate imperfect parallelism in the x direction. Similarly, the lower chip can be used to indicate parallelism error in y direction.

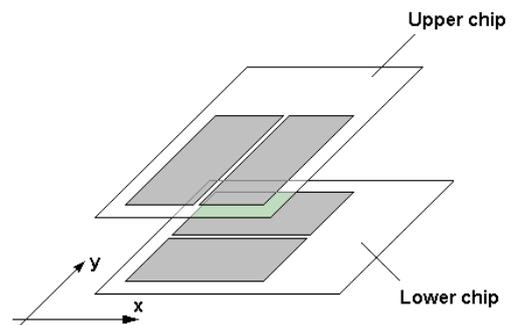


Fig.9. Parallelism control

VI. SIMULATION RESULTS

In order to find out that to what extent the measurement arrangement is sensitive to the secondary heat-flow paths excessive simulation work has been performed. One result of these investigations is shown in Fig. 10.

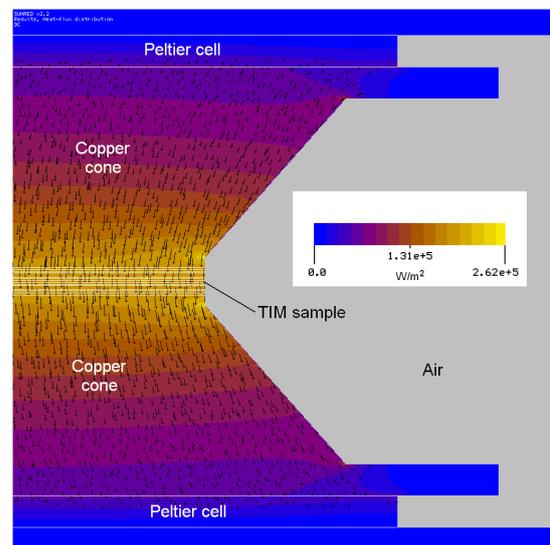
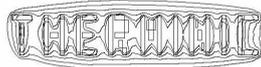


Fig.10. Thermal simulation of the sample holder

¹ And the TIM material is homogeneous



24-26 September 2008, Rome, Italy

This figure represents cylinder-symmetrical heat-flux simulation of the TIM tester sample holder. In order to achieve a vertical heat-flux, we considered adiabatic boundaries on all sides of the investigated volume and a +/- 30 W heat pumping on the Peltier cells. The maximum heat-flux through the chip is around 200 kW/m² and only 0.3 W/m² heat-flux can be observed through the air. The results also indicate 262 kW/m² heat-fluxes near the chip, in edges of the truncated copper cone. Through these excitations 46.6 K temperature difference is achieved in the whole structure which results in approximately 3.5 K in the two chips.

VII. CONCLUSIONS

New concept sample holder and evaluation electronics has been developed for static thermal resistance measurement of TIM materials. The main features of this new design are (i) the use of Peltier cells to obtain controlled heat flow through the sample and control the sample temperature, (ii) the symmetric mechanical arrangement which allows the repetition of the measurement in reverse heat flow direction, (iii) the use of integrated silicon chips both for heat flow and temperature measurement. With these new concept thermal resistance values as small as 10 mK/W are expected to be measured with an accuracy of 2 – 3 %.

ACKNOWLEDGMENTS

The authors acknowledge the help and contribution of their colleagues E. Kollár and M. Ádám. This work is supported by the NanoPack project 216176/2007 of the EU.

REFERENCES

- [1] C.J.M. Lasance, C.T. Murray, D.L. Saums and M. Rencz, "Challenges in Thermal Interface Material Testing", Proc. of 22th *IEEE SEMI-THERM Symposium*, pp 42-49, 2006.
- [2] K. Zhang, Matthew M.F. Yuen, N. Wang, J.Y. Miao, David G.W. Xiao, H.B. Fan, "Thermal Interface Material with Aligned CNT and Its Application in HB-LED Packaging", *IEEE Electronic Components and Technology Conference*, pp 177 -182, 2006.
- [3] R.N. Jarrett, C.K. Merritt, J. P. Ross, J. Hisert, "Comparison of Test Methods for High Performance Thermal Interface Materials", Proc. of 23th *IEEE SEMI-THERM Symposium*, pp 83-86, 2007.
- [4] D. Keams, "Improving Accuracy and Flexibility of ASTM D 5470 for High Performance Thermal Interface Materials", Proc. of 19th *IEEE SEMI-THERM Symposium*, 2003.
- [5] Bosch E. and Lasance C., "High Accuracy Thermal Interface Measurement of Interface Thermal Resistance", *Electronics Cooling*, vol.6,110.3, pp. 26-32.2000.
- [6] NanoPack interim report Wp 4.
- [7] M.Rencz, E.Kollár, V.Székely: "Heat flux sensor to support transient thermal characterisation of IC packages", *Sensors and Actuators, A. Physical*, Vol. 116/2 pp. 284-292, 2004