Real-Time Infrared Test Set:
System Design and Development

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ABSTRACT

During the past several years, the technology for designing and fabricating thermal pixel arrays (TPAs) using silicon micromachined CMOS devices has been developed adequately to support the development of a real-time infrared test set (RTIR) for sensors and seekers. The TPA is a custom application-specific integrated circuit device that is fabricated using a low-cost commercial CMOS process. The system architecture and development of the initial RTIR Test Set is described. The RTIR is a compact, self-contained test instrument that is intended for test and evaluation of infrared systems in the field. In addition to the TPA, the RTIR contains projection optics and electronics which drive the TPA, provide TPA non-uniformity compensation, data translation, data transformation, and user interface. The RTIR can display internal test patterns (static and dynamic), external digital video data, and NTSC video. The initial RTIR unit incorporates a 64x64 TPA to provide flickerless infrared scenes at 30 frames per second. Additional TPAs are under development with formats of 128x128, 256x256, and 512x512 pixels.

KEYWORDS: Infrared Projector, HWIL Testing, Infrared Source, Test Set, Infrared.

1. INTRODUCTION

Infrared sensors and seekers have become an instrumental part of the war-fighting capability of the U.S. military in addition to satisfying numerous industrial, civilian, and government applications. The military systems are typically used for surveillance, targeting, and tracking in war-fighting applications. These systems are frequently used where the threat platforms or operations are naturally difficult to detect in background clutter or where measures have been taken to reduce their signatures. Furthermore, the need to observe potential targets at ever increasing ranges has resulted in the development of enhanced infrared sensors and seekers of increased complexity and sophistication. Existing sensors and seekers systems have requirements for improved readiness testing to improve the probability of accomplishing their missions. One approach to achieving, in part, this goal is to provide our forces a portable infrared test set that could be used to perform pre-sortie, full end-to-end testing of missile and FLIR systems.

The key element necessary to develop a practical and cost effective infrared test set is a real-time thermal infrared scene generation device. For over two decades, researchers have investigated a wide variety of technologies for use as a real-time infrared scene generator.[1] During the past several years, the most promising technology to meet the myriad of applications appears to be the silicon micromachined resistive-array approach where each thermal pixel is created by a micro-scale resistor. The application of this technology in the development of a low-cost, real-time infrared test set for field evaluation of infrared sensors and seekers can now be considered viable and practicable as a consequence of these low-cost, high-performance thermal pixel arrays (TPA) as display devices. This technology has been developed adequately to support the development of a real-time infrared test set (RTIR) for sensors and seekers. The system architecture and development of the initial RTIR Test Set is described in the following sections. The RTIR Test Set is a compact, self-contained test instrument that is intended for test and evaluation of infrared systems in the field. In addition to the TPA, the RTIR contains projection optics and electronics which drive the TPA, provide TPA non-uniformity compensation, data translation, data transformation, and user interface. The RTIR can display internal test patterns (static and dynamic), external digital video data, and RS-170/NTSC video. The initial RTIR unit incorporates a 64x64 TPA to provide flickerless infrared scenes at 30 frames per second. Additional TPAs are under development with formats of 128x128, 256x256, and 512x512 pixels.

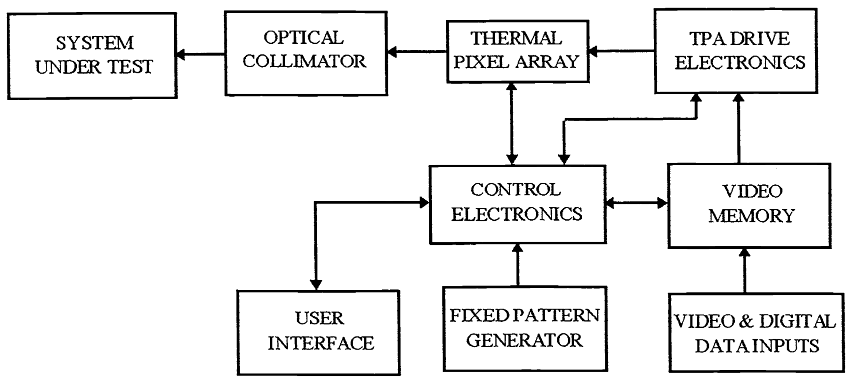

Figure 1. Basic RTIR Test Set block diagram.

The basic block diagram for the RTIR Test Set is shown in Fig. 1. Aspects of the function, design, and evaluation of each of these blocks will be presented in the following sections.

2. THERMAL PIXEL ARRAY

CMOS-compatible thermal emitters have been reported previously.[2] These devices are fabricated in a standard commercial CMOS foundry with an additional maskless anisotropic silicon wet etch that is carried out after the full CMOS process is complete.[3,4] The thermal emitter device comprises a polysilicon resistive heater that is encapsulated in glass. The glass also provides the mechanical support for the structure. The glass and polysilicon films are from the standard 2 μm CMOS process. The glass is patterned with four openings that expose the substrate to a chemical etchant. These openings are patterned in order to remove the substrate silicon directly beneath the heater and to provide thermal isolation of the device. The silicon etchant removes the substrate material forming a pyramidal cavity under the heating element.

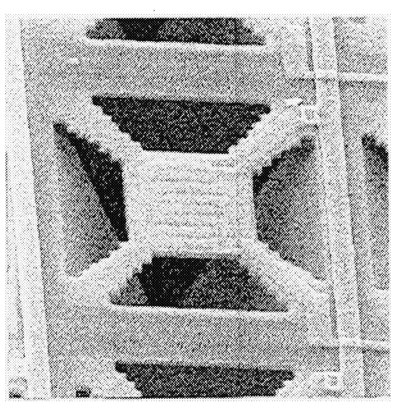

Figure 2. SEM photomicrograph of an early CMOS microheater. The size of the pit is 150 μm on a side.

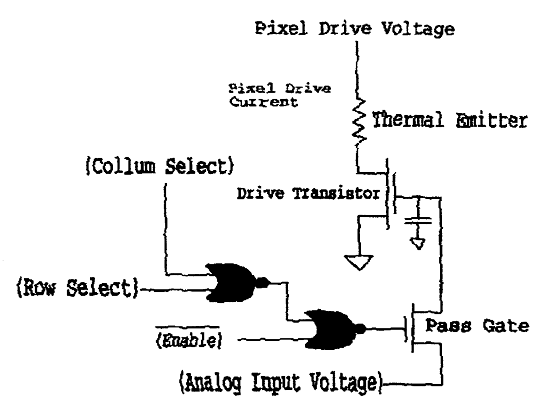

Figure 3. Schematic representation of the pixel drive and control circuit used in the TPA design.

Figure 2 shows an SEM photomicrograph of an early thermal emitter device. The size of the pit in this early device is 150 by 150 μm (pits for current OETC TPAs are about 80 μm by 80 μm). The high thermal isolation of the device allows its heating to high temperatures with low input power. The low thermal mass of the device allows fast transient control of its temperature. These devices can be switched from ambient to hundreds of degrees above ambient in times on the order of 1 ms or so which is more than adequate to satisfy the requirements of thermal display operation at video frame rates of over 100 Hz.

These thermal emitter elements can be configured into arrays to form a thermal display. Each of the thermal emitter elements would form a single thermal pixel in the display. The fabrication methodology to realize the thermal emitter elements is completely compatible with digital and analog CMOS circuits.[5] Circuits to drive and control the temperature of the thermal emitter elements in the array can be designed around the perimeter of the devices as shown in Fig. 3. Thermal displays with arrays of 16x16, 32x32, and 64x64 thermal pixel elements have been designed, tested, and shown to be fully functional. TPAs with 128 by 128 (TPA-128) thermal pixel elements, as shown in Fig. 4, have been fabricated and are being tested while a TPA having a 256 by 256 (TPA-256) format has been designed and awaits fabrication in the near future. An important aspect of the post-foundry fabrication process is the etching of the chip.

The procedure used to post-process the wafers received from the foundry into functional, packaged TPA modules comprises four basic steps, viz., sawing (dicing) the wafers into TPA chips, etching the chips to release the pixel heaters, mounting each chip in a chip carrier or header, and wirebonding the chip pads to corresponding carrier pads. The etchant is a solution of tetramethylammonium hydroxide (TMAH), dissolved silicic acid (SA, which is powdered silica), ammonium perxyodisulfate (APODS, also known as ammonium disulfate), and deionized (DI) water in a variation of the procedure described by Klassen.[6] Once the chip is etched and the TPA module is prepared, a variety of electrical tests are performed before proceeding to the radiometric evaluation. Although only a small number of TPA-64s were prepared, the yield appears to be quite acceptable.

For TPA displays, a mixed serial-parallel architecture provides a moderate data bandwidth requirement that is accommodated by using an encoded row-address and refreshing the pixels of each row of the array in parallel. Depending on the chip carrier/header pin-out constraints, all the column-inputs can be applied in parallel or several parallel inputs can be multiplexed to the columns. This architecture was adopted for all TPAs with formats of 32x32 and greater. The TPAs utilize current as input signals to set the radiometric output from the pixels since current signals are more noise-immune than voltage inputs.

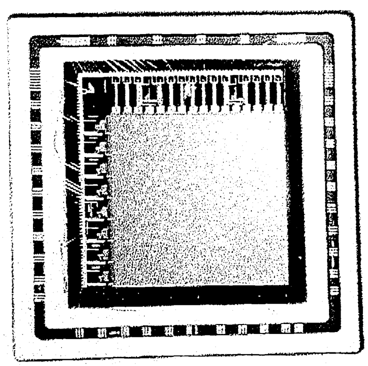

Figure 4. Photograph of a thermal pixel array having a format of 128 by 128 pixels.

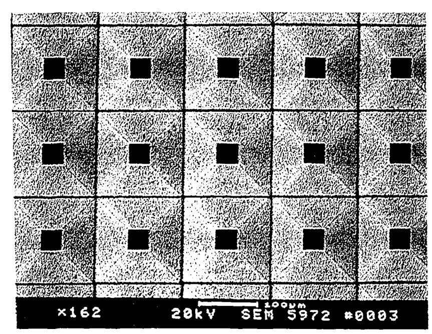

Figure 5. Optical augmentation device micromachined from silicon.

Design of the large arrays requires a thorough CAD design-verify cycle in order to assure a viable array. The design proceeds from a physical layout of an array of mixed-signal electronic cells and custom miromechanical pixels to a schematic of the layout. A design-rule-check (DRC) is performed on the completed layout. Following a successful DRC, a netlist of the array is extracted from the layout. The netlist derived from the layout is cross-checked against the netlist derived from the schematic in a layout-vs.-schematic (LVS) check. If the LVS is successful, the schematic is manipulated and netlist is simulated for a final test for electrical integrity such as signal continuities, shorts, or opens in the design. When the design passes this final check, it is then ready to be submitted to the foundry for fabrication.

TPAs have been successfully fabricated and tested and have been evaluated with a wide array of input signals and studied with an IR camera. Numerous fixed patterns, stored in memory or transferred remotely, were used to study the various addressing, input, and multiplexing operations of the arrays. Video input is a most convenient means for providing the array with display data. The control electronics for the TPA-64 was designed to accept video-format display data to exercise the array in real time. Live image from a video camera have been successfully displayed in real-time on the array.

The TPA chip is mounted in a custom carrier designed to allow the chip to be temperature stabilized using a thermoelectric cooler. The carrier and corresponding support PC board are located inside of the TPA enclosure. This enclosure provides for the operation of the TPA in a near-vacuum environment. From measurements made at NRaD and NIST, the conductive heat loss through the air becomes negligible for pressures less than a modest 100 mTorr. For the same electrical current input to the heater, the observed signal in the 3–5 μm band increase by about a factor of 9 when the air was removed.

A means to enhance the apparent radiometric output of the thermal pixels has been investigated. The heater element radiates flux over approximately a hemisphere (2π sr). Because the collection solid angle of the projection optics is significantly less than 2π sr, much of the radiated flux is not collected. Since the heater element area is about 20% of the area "assigned" for a pixel, an optical augmentation device[7] which is attached to the TPA was developed to capture much of the uncollected flux and channel it into a solid angle more closely matching the projection optics. As a consequence, the flux is spread over an area approximately the same as the pixel area. Figure 5 shows a photomicrograph of one realization of the optical augmentation device. Recent measurements indicate the device function as predicted by the computer model. A full-scale optical augmentation device is presently being fabricated for integration with the TPA-128.

To assist in optimizing the design of the TPA-64, the transient thermal response of a single pixel heater element was analyzed by using a finite element model (FEM). The ANSYS© finite element analysis program was used for the analysis. Because of symmetry, only half of the heater element was modeled. Modeling only half of the element helped to decrease solution time since the model comprises over 3,000 three-dimensional, eight-node solid elements. Each node has one degree of freedom, viz., temperature. As a consequence of the extremely small dimensional parameters (some layers of material are only 0.4 μm thick) and the fast response of the heater element, the solution time step-size requirements were as small 10^{-7} s. This allows the thermal response of the heater element to be visualized at virtually any point in time.

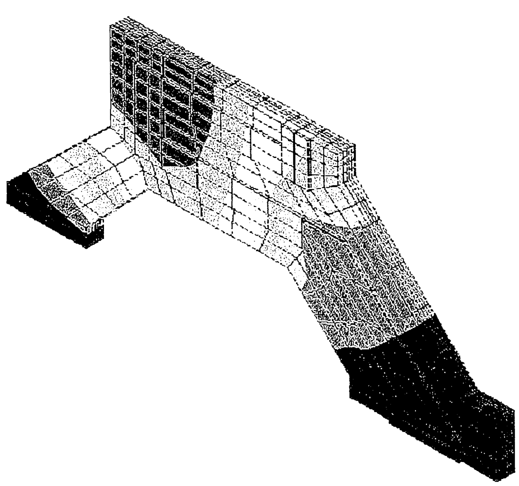

Figure 6. Temperature contour plot of the heater element

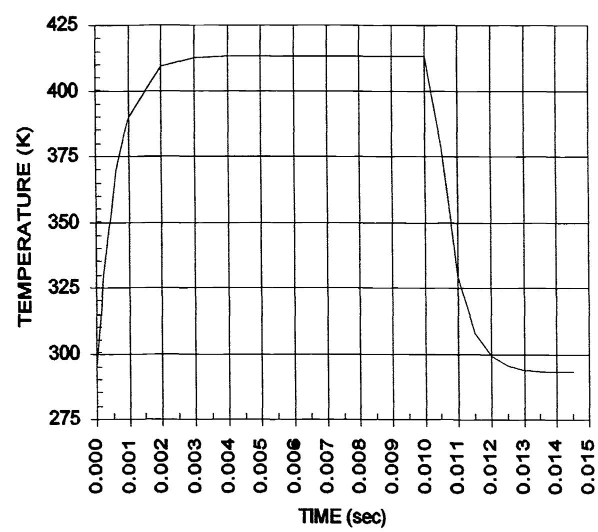

Figure 7. Transient thermal response of a typical node.

The results of the thermal analysis includes transient thermal response, temperature contours, and total power emitted by radiation. The radiant flux was calculated by having the upper surface of the "trampoline" portion of the pixel heater element radiate to a body fixed at room temperature with an emissivity of 0.80 and a form factor of 1.0. The temperature contour plot shown in Fig. 6 presents the trampoline portion of the heater element operating in its steady-state condition with 1.5 mW of power input. The analysis assumes the heater element is operating in vacuum. The hottest region is located in the upper left region of the figure. The power buss extends along the right leg while the left leg is used for support.

The rise time (10–90%) of the heater element is about 2 ms and the steady-state condition is reached in about 3 ms. The transient thermal response of a typical node versus time is presented in Fig. 7. The input power to the heater is turned off at 10 ms. The fall time is about the same as the rise time. The model is generally consistent with measurements made at NIST in the 3–5 μm band. The fall time was observed to be faster than the model predicted since the heat rapidly disperses over the trampoline at power turn-off which quickly reduces the radiated flux in the 3–5 μm band.

Certain limitations exist in the range of possible heater geometries due to the CMOS process used and the specific set of available design rules. An accurate model was developed to determine the characteristics of any heater configuration. This provided a cost- and schedule-effective means to explore various designs to improve the heater performance of the TPA-128 and future TPAs. The basic goals in developing an enhanced heater configuration were to achieve a more uniform radiating area, maximize the radiating area, and maximize the temperature for a given electrical input power. The model for the resultant enhanced heater design indicates a notable effective temperature increase, the temperature uniformity improves dramatically, and the total or broadband radiated power increases significantly. The predicted response times are slightly longer than for the TPA-64. Measurements of actual heater will be made presently.

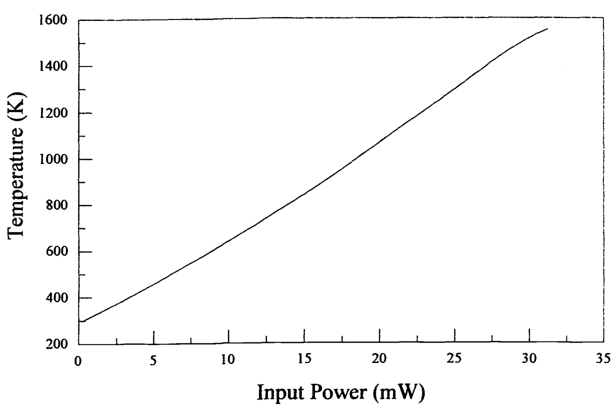

Figure 8. Electrical temperature versus input electrical power for the OETC thermal pixel heater element with the chip maintained at ambient temperature.

Determination of the digital encoding requirements for the TPA drive signal necessitates consideration of one of the system specifications for the RTIR Test Set. It states that the instrument provide 1 °C temperature resolution throughout the designated operation range of ambient to 573 K. Prior papers have reported that the pixel heater temperature is approximately linear with input electrical power.[8,9] Recent measurements at NIST of the TPA-64 heater element illustrate this nominal behavior as illustrated in Fig. 8. From the measurements, the slope of the curve is about 37°C/mW of electrical power input to the heater. Since the TPA drive signal is a current, the relationship between the heater temperature and current is roughly quadratic. Also, the heater resistance increases about 30% over the operational range. From the NIST measurement, the heater temperature increase per mA increase in current is about 17.7 °C/mA at 300 K and about 186 °C/mA at 573 K.

It should be noted that the "electrical temperature" is determined by heating the entire chip on a hot plate and measuring the resistance of the heater as a function of temperature. The temperature coefficient of resistance of the polysilicon heater element is determined from this data. The heater element is at a uniform temperature in this case. Consequently, the electrical temperature and radiometric temperature will be somewhat different due to the non-uniform temperature of the heating element when used in its normal operational mode.

The maximum current increment at the heater element to assure that the least significant bit corresponds to an incremental change in temperature of 1 °C when the device is about 570 K is 1/186 mA or 5.4 μA. Dividing the heater current under the 570 K condition by 5.4 μA implies that 10-bit words are needed. The resolution at 300 K is therefore about 0.08 K. It should be understood that the TPA drive signal currents are amplified on the TPA chip and are notably less than the heater currents. In order to provide adequate adjustment for pixel-to-pixel non-uniformity, additional temperature range, and improved temperature resolution, the data word size was selected to be 16 bits. Depending upon how the user desires to employ the RTIR Test Set, the video/digital input data will be limited to 12–13 bits in general.

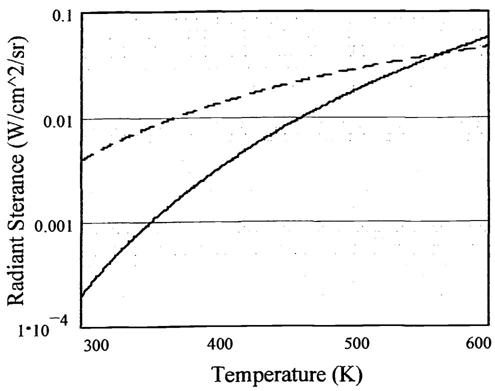

Figure 9. Radiant sterance in the 3–5 μm (solid curve) and 8–12 μm (dashed curve) spectral bands as a function of temperature.

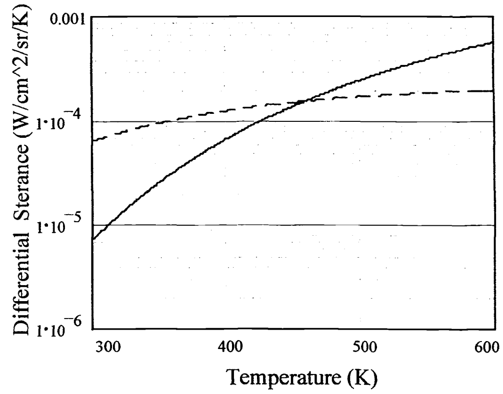

Figure 10. Differential radiant sterance in the 3–5 μm (solid curve) and 8–12 μm (dashed curve) spectral bands as a function of temperature.

The stressing case regarding word size for signal data encoding is a consequence of 3–5 μm band radiometrics. The radiant sterance (L) in the 3–5 μm and 8–12 μm spectral bands as a function of temperature is illustrated in Fig. 9. It is evident from this figure that the dynamic range of the sterance in the 3–5 μm band is significantly greater than in the 8–12 μm band. The 573 K requirement implies that the ratio of L(573 K)/L(300 K) is about 250 in the 3–5 μm band and about 11 in the 8–12 μm band. The differential sterance (dL/dT) is shown in Fig. 10. The value varies almost two orders of magnitude in the 3–5 μm band while less than a factor of 3 in the 8–12 μm band Figure 9 also provides insight into the data transformations necessary for when sterance data are input into the instrument.

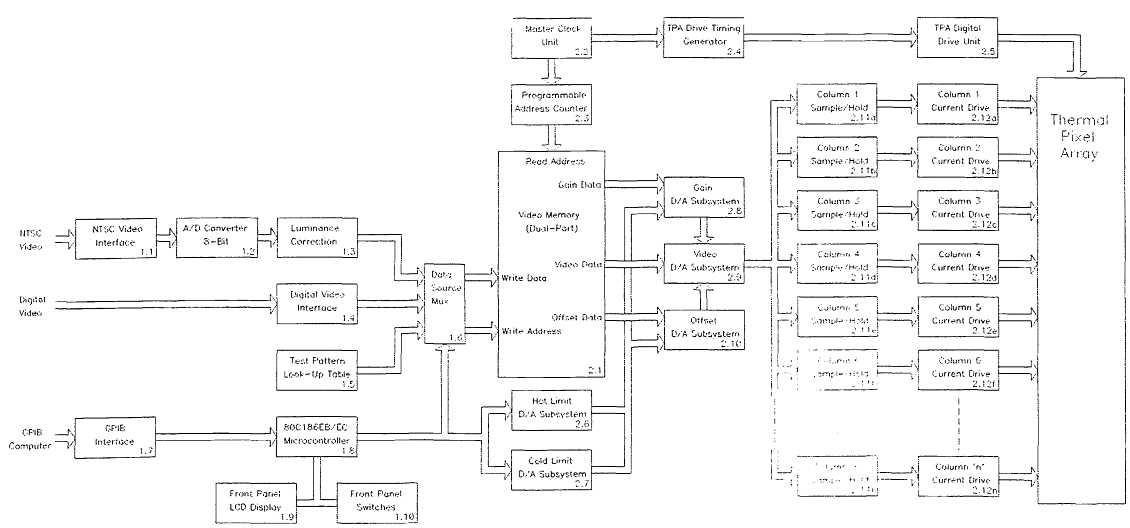

Figure 11. System Partitioning of the RTIR Test Set.

3. SIGNAL PROCESSOR

The RTIR Test Set electronics system consists of a number of modules arrayed in a reconfigurable and expandable architecture to allow for logical system growth. The system utilizes multiple high-speed data pipelines, with a 16-bit wide digital data path throughout. Full 16-bit precision is maintained throughout the data path, yet provides the ability to accept data from sources with less than 16-bit per pixel precision. The digital data path ends with 16-bit digital-to-analog converter sections which provide the analog drive to the Thermal Pixel Array. Modular system partitioning provides a straightforward means to increase system capability by adding or substituting modules with new data sources, processing means, or system modes. The current RTIR Test Set system partitioning is shown in Fig. 11.

Data may be input from one internal or external source at a time. An internal fixed pattern generator provides up to 64 static 16-bit gray-scale patterns which may be displayed. A real-time video port is provided to accept externally produced data and convert it from RS-170/NTSC into 8-bit words. Externally supplied 16-bit data may be applied to the digital video port at a rate of up to 12 megawords per second. Fixed patterns, which are externally generated, may be loaded into the test set through the GPIB port. Other data sources may also be included by adding or changing system modules.

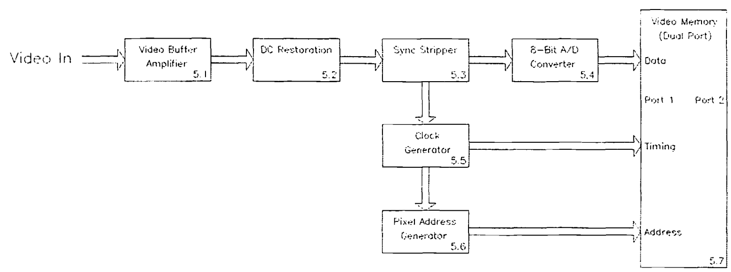

Figure 12. RTIR Test Set Video Input Subsection

As shown in Fig. 12, the video input provides the capability to display live or prerecorded video on the TPA. The video source may be either in the RS-170/NTSC or PAL formats. For any video source, only the luminance information is displayed, and any chrominance information is ignored. Because the video formats have a 4:3 aspect ratio and the TPA format is square, the video subsystem samples a square window from the input video. This window covers approximately 75% of the area of the original image, and may be swept vertically and horizontally to any part of the original image. The video is digitized with a high-speed sampling 8-bit analog-to-digital converter. The digitized video can then be modified with a luminance correction function, selected from among up to 128 internally stored functions, or from a user-defined correction function which may be downloaded through the GPIB port. In this way, video recorded in virtually any arbitrary temperature or sterance scale can be accurately displayed on the TPA.

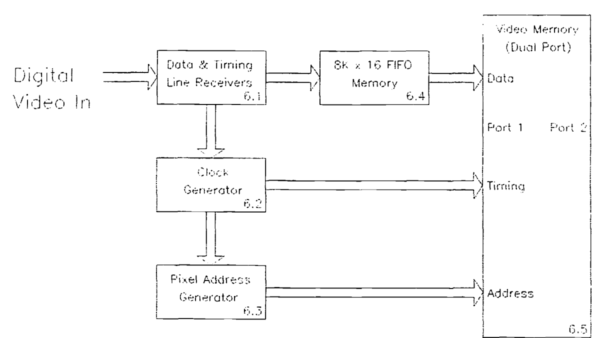

Figure 13. RTIR Test Set High Speed Data Port

The internal fixed pattern generator can hold and display, one at a time, up to 64 patterns,. These patterns have a full 16-bits per pixel of precision for TPAs having formats of 64x64, 128x128, or 256x256 pixels. These patterns are stored in non-volatile memory and, consequently, do not have to be reloaded at power-up. Fixed patterns may be scaled to arbitrary temperature ranges by setting the hot and cold limits in the TPA drive circuitry which is described later.

The high-speed data port input, presented in Fig. 13, can accept parallel digital data of up to 16 bits per pixel at a rate of up to 12 megawords per second with planned growth capability to 24 and 48 megawords per second. Pixel data words are accepted in raster scan order starting at the top left corner of the image, scanning rows and then columns. There is no requirement that data be synchronous to the TPA operation. However, signals are available at the port to synchronize the input data to the TPA if this is required to eliminate temporal aliasing. The TPA is flickerless, but can change radiant output very quickly. Some infrared systems may require this synchronized data-display feature. Images input through the high-speed data port may be scaled to arbitrary temperature ranges by setting the hot and cold limits in the TPA drive circuitry.

For externally generated data of whatever source, the image is buffered through a dual port memory which decouples the input timing from the output timing. The address and data busses for the dual port memory input and output are entirely separate, and the memory devices support this with concurrent noninterfering write and read cycles. Thus, there is no arbitrarily defined timing restriction on input data asynchronous/synchronous input and the input and output subsystems may be run entirely independently of each other while producing full TPA display. There is the possibility of temporal aliasing and minor visible artifacts in this asynchronous mode and a synchronous mode is also provided. Signals at the high-speed port interface provide accurate timing information which allows the input data to be synchronized to the TPA output, if required.

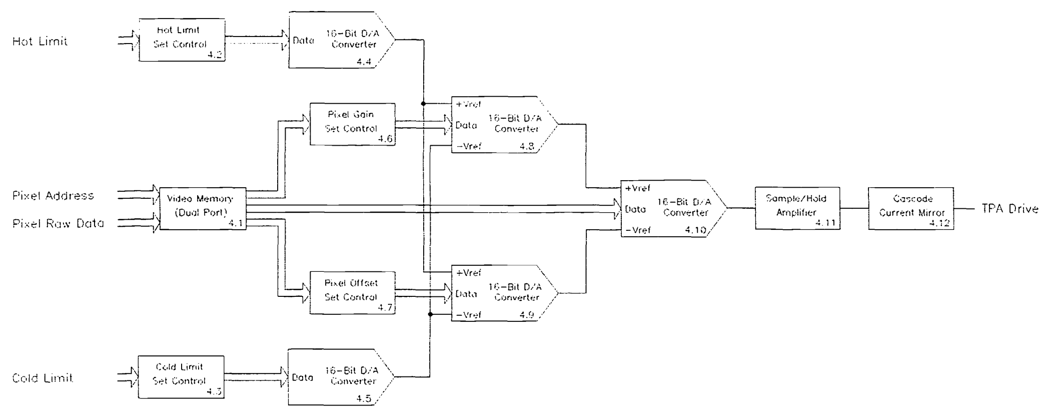

Figure 14. Nonuniformity Correction Analog Signal Processing

Minor variations in responsivity of individual pixels in the TPA require the use of correction circuits to tailor the drive level of each pixel. This nonuniformity correction (NUC) function in the Demonstration RTIR Test Set is accomplished by storing correction coefficients for each pixel and applying these in real-time to the drive of the respective pixels in sequence. The current design utilizes pixel-by-pixel dynamic linear-correction to compensate for pixel-to-pixel variations. This is applied using multiple banks of memory which supply independent 16-bit values for the video level, offset, and gain for each pixel. These values drive digital-to-analog converters and an analog signal processing circuit which performs the addition and multiplication functions as shown in Fig. 14. In subsequent signal processor implementations, digital signal processors (DSP) will be used to perform more sophisticated nonuniformity correction functions.

The control signals to the TPA comprise multiplexed analog column current drives and digital timing signals. The pixel data, which are stored in the dual port video memory in raster scan order, are read out by a programmable address counter in an address order which has been sequenced to provide the required column order multiplexing. The TPA drive timing generator provides the timing signals for both the drive analog electronics and the TPA itself. The drive electronics generate the analog pixel values sequentially and utilize sample and hold circuits to allow the analog data to be presented to the TPA as 16 simultaneous column drive signals. Wilson current mirrors are used to convert the drive voltages into the currents which are input to the TPA. This parallel analog data path maximizes data throughput while maintaining high accuracy.

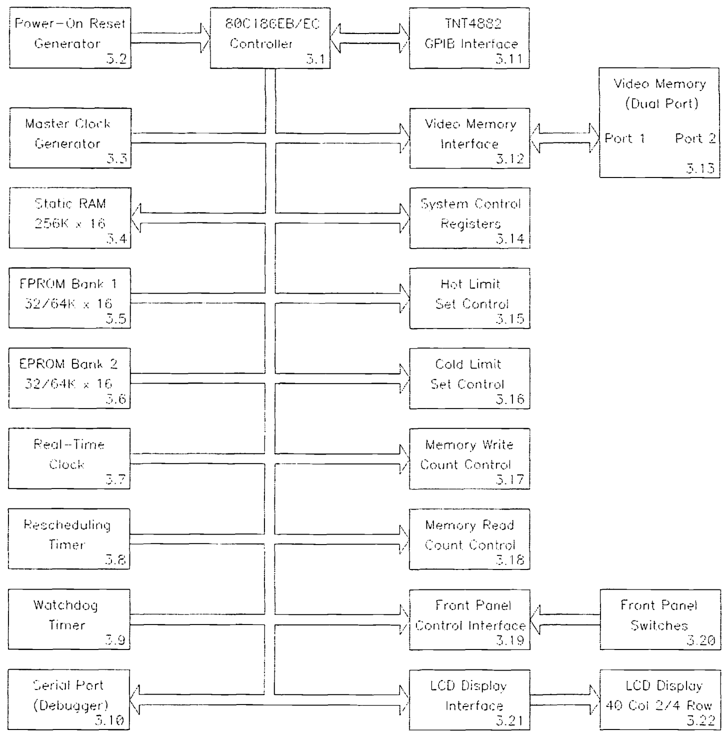

Figure 15. Microcontroller and its associated hardware.

All system functions are supervised by a microcontroller which is controlled and monitored through an on-board control panel. The microcontroller and its associated hardware are shown in Fig. 15. This microcontroller allows the instrument to stand alone and to be used without any external control devices. This enhances portability since the instrument can be transported and operated without the additional size and weight of external hardware. Many functions are controllable through the internal firmware including such preprogrammed system functions as selecting the video and internal fixed pattern modes, selection from up to 64 preprogrammed internal fixed patterns, selection of preprogrammed internal video luminance correction curves, setting hot and cold temperature limits, and setting the TPA substrate temperature. The microcontroller has the resources to directly control system modes, and to directly inspect and manipulate the contents of video memory. Full system control from external computer systems is available through a GPIB port implemented with a National Instruments TNT4882 chipset.

The GPIB port provides the means to control the RTIR Test Set from an external computer or test system. By this means it is possible to integrate the RTIR Test Set into automated test regimes, and perform automated testing of units under test. All locally controlled functions described above are available for remote operation. Additional functions available through remote control include providing a means of automated calibration of the test set; programming of the nonuniformity correction subsystem; advanced functions and data manipulation; loading externally generated fixed patterns; loading externally generated video luminance correction curves; setup of high speed data transfer operations through the high speed digital port; and display of frames of data taken from any data source, internal or external.

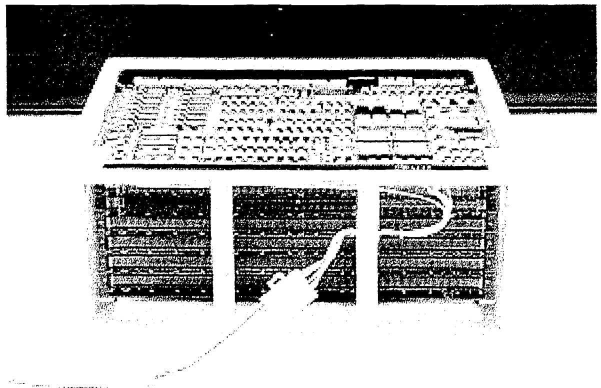

Figure 16. RTIR Test Set Modular Electronics Card Rack

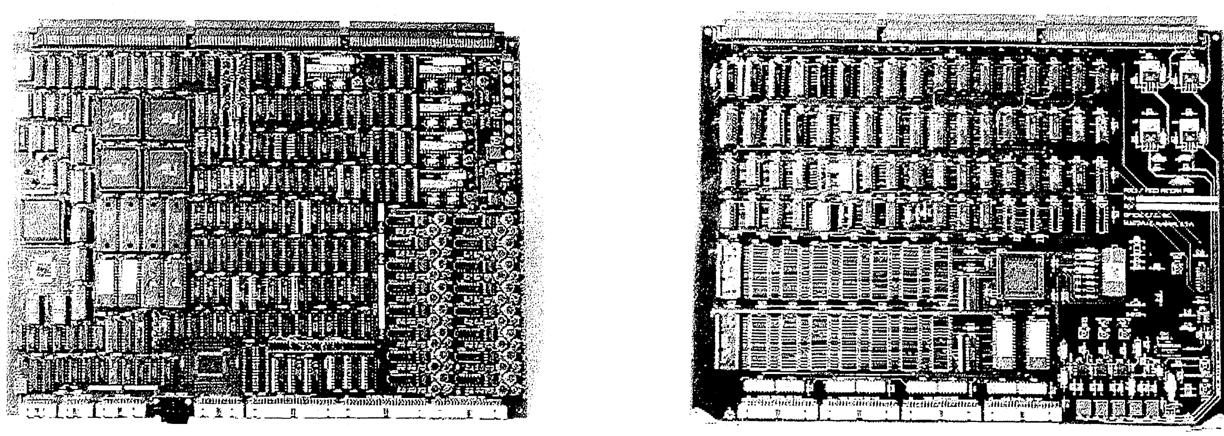

Figure 17. Typical RTIR Test Set Printed Wiring Boards

The RTIR electronics package comprises a card cage and a small number of printed wiring boards which can be changed depending upon the application and can be customized to accommodate user requirements. The high-reliability two-part backplane connectors have 540 contacts apiece which allows space for multiple wide data and address busses. Figures 16 and 17 show photographs of the card cage and two representative RTIR Test Set printed wiring boards. Proper attention has been paid to digital and analog signal integrity to insure that each system will work as designed. The signal processor for the Demonstration RTIR Test Set has been fabricated and successfully tested. The use of a full 16-bit system has necessitated that special techniques be used to maintain the maximum dynamic range with the analog subsystems in close proximity to the digital electronics. Manufacturability and testability were key considerations in the design process including such measures as maximizing the use of industry standard parts and procedures, placing all parts on a standard grid, allowing proper access space for each component, providing test ports on all major logic sections, allowing the use of external clocks and resets driven from the card edge, and including the logic on each card to allow the memory and logic to facilitate the determination of its internal type and configuration information from the card edge. The design of the electronics package allows it to be manufactured and used with minimum acquisition and life-cycle costs.

4. USER INTERFACE

As previously discussed, the RTIR Test Set is intended to be easily used by military personnel in an operational environment as portable test equipment. Consequently, the user interface needs to be functional, self evident, and comprehensive. The RTIR Test Set actually provides two user interfaces denoted as "Internal" and "Computer." The Internal Interface is located on the housing of the instrument and comprises an LCD or gas-discharge display and six push button switches. By utilizing this interface, the user may select a data source, activate an internal test pattern, select the temperature or radiance radiometric mode, adjust the radiometric parameters of the test pattern, select the non-uniformity compensation function, engage/disengage TPA, transfer control to an external computer, and shut the system down. In addition, the interface provides for input of user identification and password as a means for assuring authorized operation. The LCD display also provides the user with necessary information regarding the status of the RTIR Test Set.

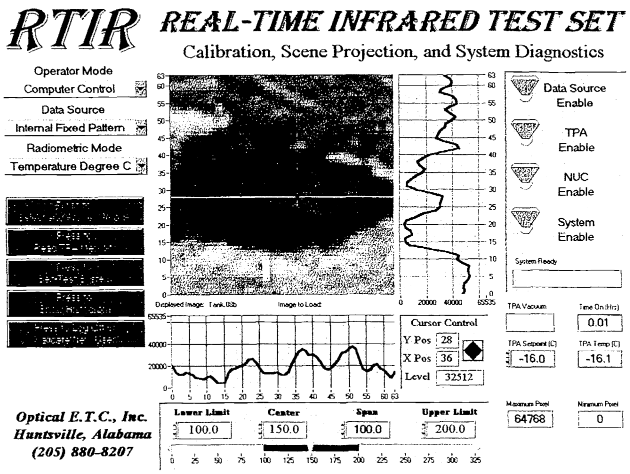

Figure 18. Principal operating panel for the RTIR Test Set.

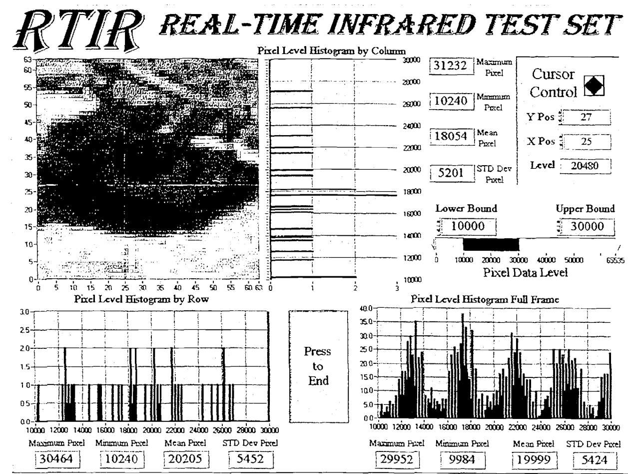

Figure 19. Data analysis panel for the RTIR Test Set.

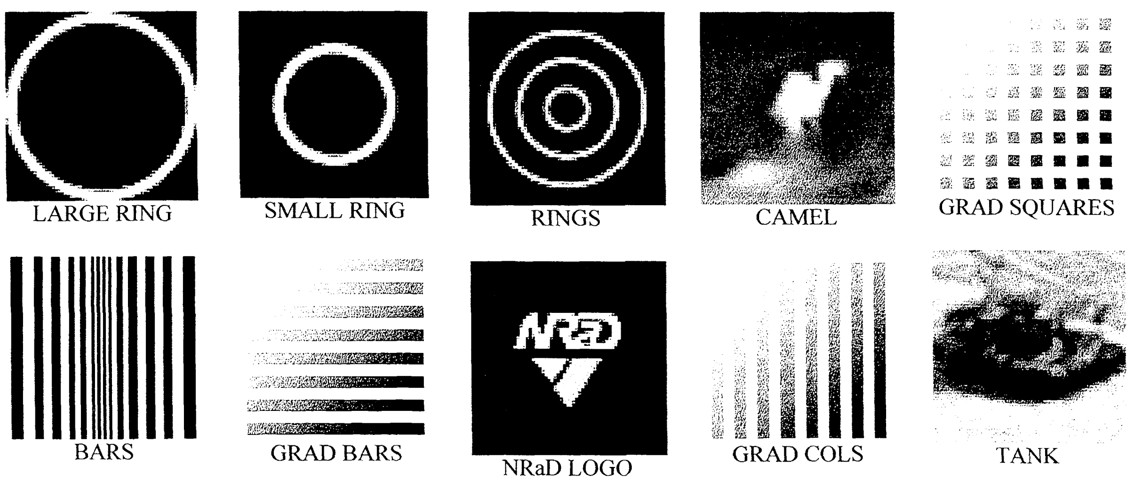

Figure 20. Representative fixed patterns.

The Computer Interface provides the user a broad-featured graphical interface that allows normal operation, calibration, and support maintenance of the RTIR Test Set. The interface was developed using the LabVIEW® software development program for operation on a typical laptop or desk top PC using Windows 95. The computer is connected to the instrument through a GPIB port. Using LabVIEW to develop the interface as a virtual instrument has several advantages such as rapid software development, no hardware development, multiple control and display panels, high extensibility, and cost effectiveness. When the system is turned on, the RTIR Test Set senses if the computer is attached. If so, then a log-in panel is displayed to determine appropriate authorization. After successful log-in, a system test is performed and the results are displayed for the user. The principal operating panel, shown in Fig. 18, is displayed next. The actual panel makes use of color to enhance its utility. The user may choose several operational modes such as computer, internal, calibration, and maintenance. A data source is selected from RS-170/NTSC video, formatted digital data, custom input digital data, internal fixed patterns, and external fixed patterns. The radiometric mode can be set to temperature, in Kelvin or °C, or radiance.

On the right hand side of the operating panel, the user has a collection of switches to control the enabling system, data source, TPA, and non-uniformity compensation. Below these controls, a set of indicators and inputs provide a means to adjust the TPA substrate temperature and monitor the status of the TPA enclosure vacuum. In the center of the panel, a display is provided to allow the user to preview a set of data, view data being displayed, measure the value of any pixel by moving the cursor, and plot data along the cursor lines. The display and controls located near the bottom of the panel allow the user to adjust the temperature/radiance range of the fixed patterns. This feature is useful in such tests as MRT. It should be noted that the display does not show the video or digital data input to the RTIR Test Set in real time; however, the user can command the system to grab a frame of data and display it without disrupting the normal operation of the test set.

A set of push buttons are provided on the operating panel that allow the user to select various functions such as to acquire a frame of data from the RTIR Test Set video memory, perform a self-test, analyze the data for display, and to log off or sign on another user. One button selects the analysis panel, denoted as "Press to Show Histogram," which provides a means for the user to examine the data being input to the system. The analysis panel is shown in Fig. 19. It contains a visual display of the data, a means to measure the value of any pixel by moving the cursor, a histogram of the data along each cursor line, and a histogram of the data comprising the entire frame of data. In addition, the minimum pixel value, maximum pixel value, mean value, and standard deviation are displayed for each of these three histograms. The user can also select upper and lower bounds for the data. The analysis panel provides the user a tool to determine if a frame contains any unexpected data, what range of values are contained in the frame, etc. The analysis can be performed on the acquired data frame while the real-time data continues to be displayed by the TPA. As previously explained, the RTIR Test Set can provide up to 64 predefined fixed patterns. Figure 20 contains a representative sample of these patterns.

5. TEST SET CONFIGURATION

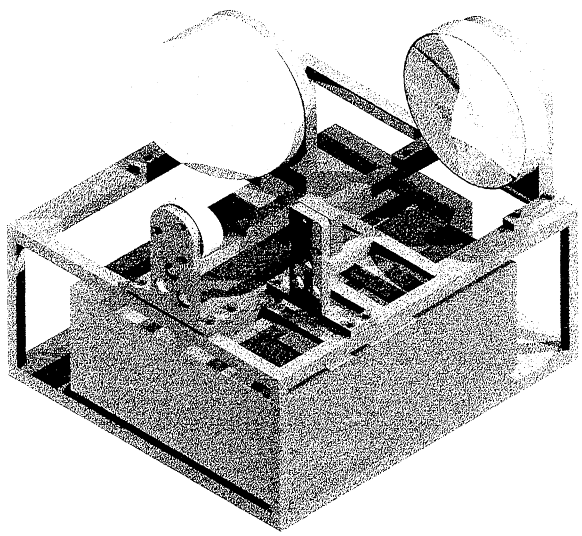

Figure 21. Basic physical configuration of the RTIR Test Set.

The RTIR Test Set being developed is intended for use in both field and laboratory environments and, consequently, needs to be reasonably small, light weight, self contained to the extent practicable, and portable. Figure 21 illustrates the basic physical configuration of the instrument which is approximately 500 mm wide by 500 mm high by 690 mm deep. The lower portion of the unit contains the power supply, signal processor, and other associated items. The optical collimator, TPA and its enclosure, and additional electronics and baffles (not shown) are located in the upper portion. Many systems that may utilize this test set require a reasonably wide field-of-view (FOV). For most applications, an active FOV of 4° by 4° to 5° by 5° was determined by potential user survey to be adequate. Since the test set may be used by systems operating in the 3–5 μm or 8–12 μm spectral bands, an all-reflective collimator design was selected and is presently being fabricated.[10] The collimator is a three-mirror off-axis configuration operating at F/4, having a focal length of 600 mm, and an exit pupil diameter of 150 mm which is located over 350 mm in front of the test set. This pupil position allows ease in matching the spatial locations of the pupil of the unit under test and the RTIR Test Set. The optical performance is essentially diffraction limited in both spectral bands over the entire field of view.

For initial testing and the Demonstration RTIR Test Set, a refractive collimator for the 3–5 μm band was fabricated. The lens has an effective focal length of 235 mm, F/# of 10.6, pupil diameter of 22 mm, pupil relief of >50 mm, total FOV >5°, and near diffraction-limited performance. The lens is about 225 mm long and has a diameter of 70 mm.

6. CONCLUSION

The Real Time Infrared Test Set will provide a compact, field portable device for evaluating performance of thermal infrared sensors and seekers. This capability is now viable due to development of the Thermal Pixel Array. This CMOS device provides a cost effective thermal scene simulation capability. Development of the entire system as well as design progression of the TPA has been presented. Measured performance of the 64x64 TPA shows that the commercial CMOS process can be used to develop a low-cost RTIR system. Performance of the electronics subsystems developed to date also demonstrates a system that provides a wide variety of functions such as input and output transfer function capability and pixel non-uniformity correction. A menu driven user interface and additional PC interface provides the capability for operation, calibration and system configuration. Planned upgrades will provide RTIRs with increased TPA formats of 256x256 and 512x512.

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 In this report, commercial equipment, instruments, and computer programs may be identified to specify the procedure adequately. This does not imply recommendation or endorsement by NIST, nor does it imply that the equipment or program is the best available for the purpose. This technology may be the subject of one or more invention disclosures assignable to the U.S. Government. Licensing inquiries may be directed to Mr. Harvey Fendelman, Legal Counsel for Patents, NCCOSC, Code D0012, San Diego, CA 92152-5765.

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